From Microelectronics to Nanoelectronics

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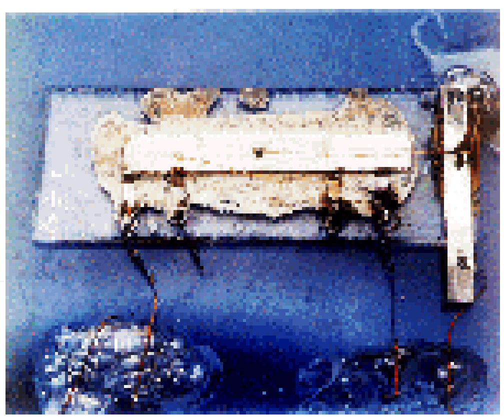
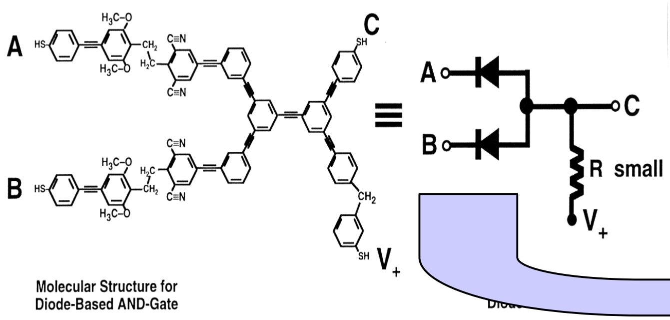
Overview

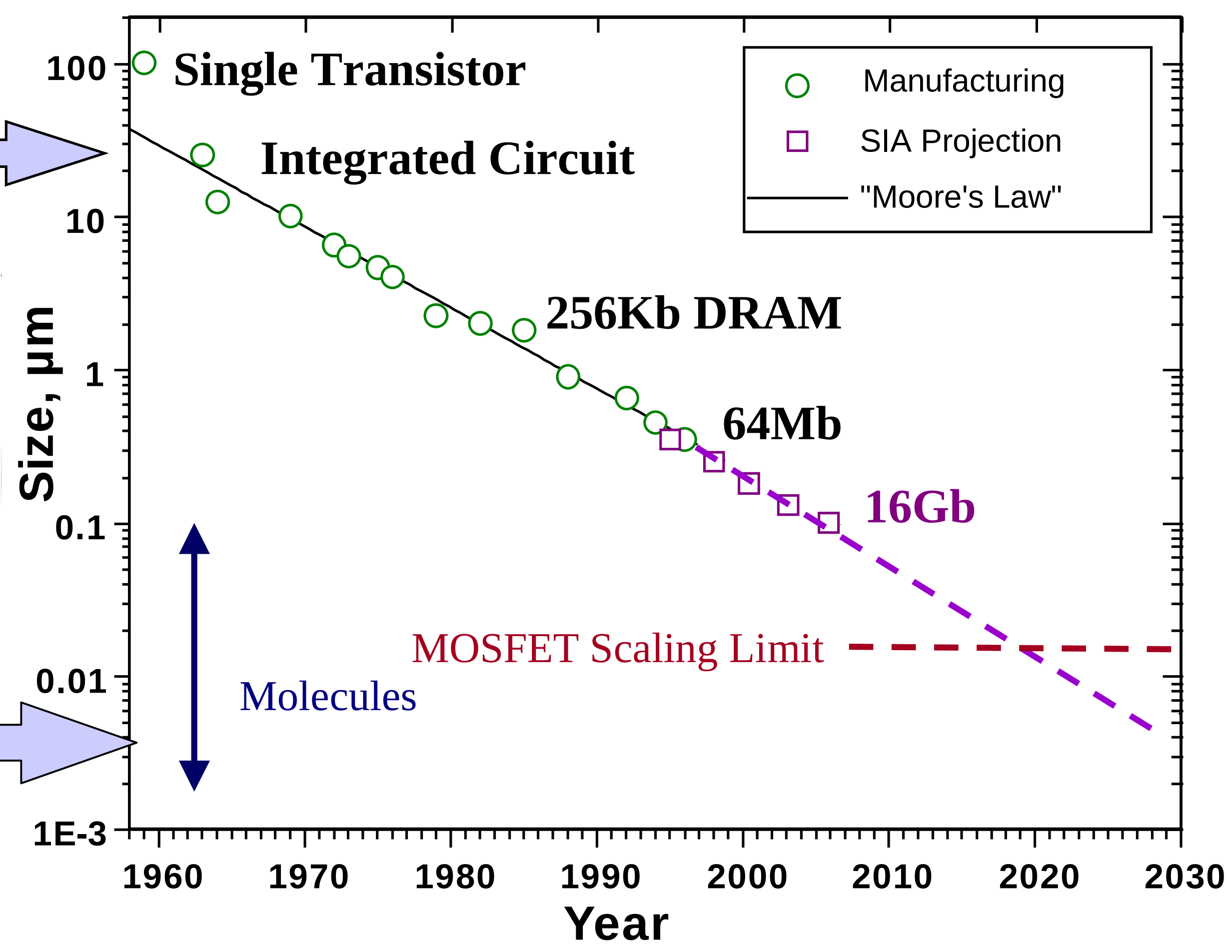
- Microelectronics is becoming Nanoelectronics
  - 18 nm transistors
- Challenges and Opportunities
  - Terabit circuits
  - Patterning
  - The molecular electronics approach
  - Designer materials
  - Integrated nanostructures

Microsystems Length Scales

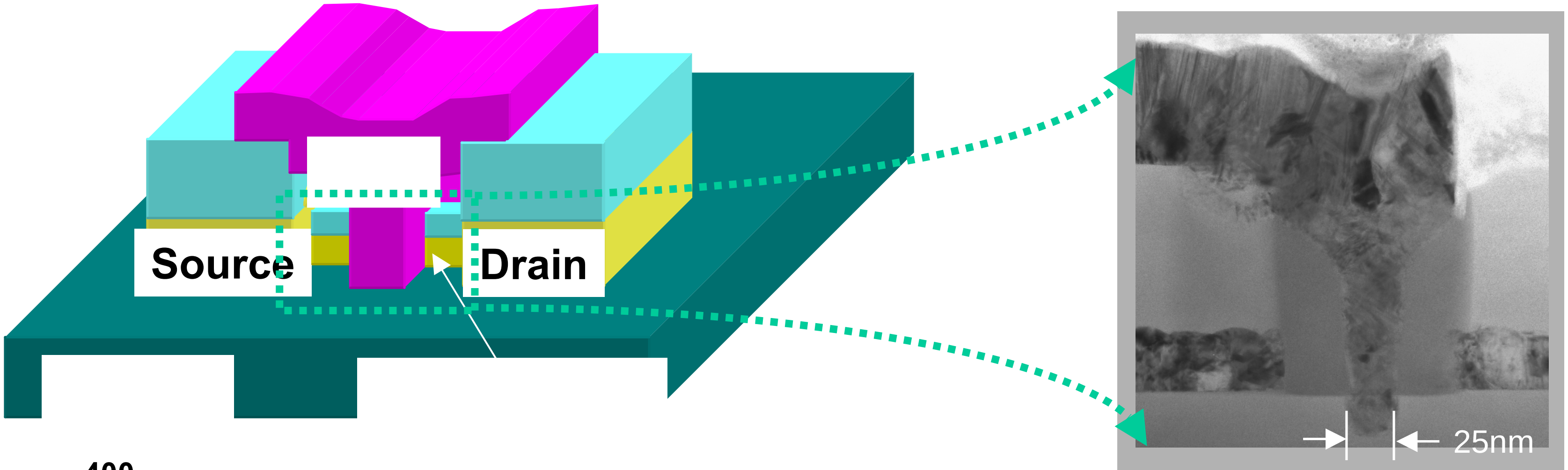
- Si scaling limits: one switch per ~100,000,000 atoms
- Molecules are multifunctional: one operation in ~100 atoms
  - Logic Element, Memory, Sensor

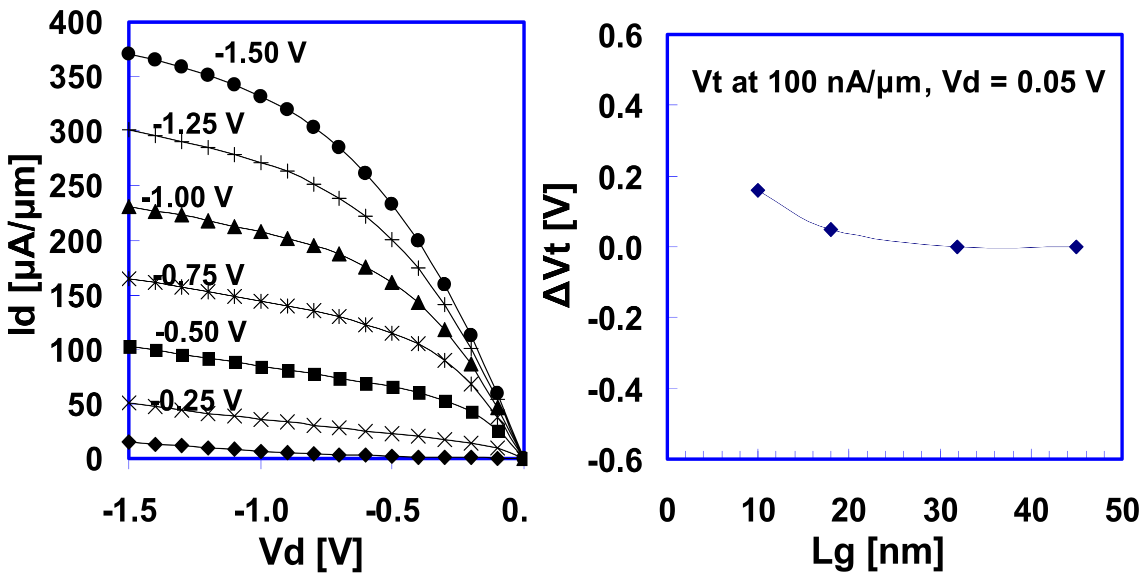






The 18 nm Transistor



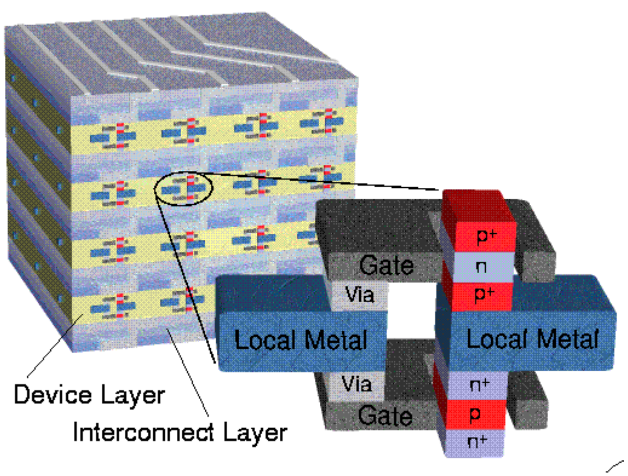


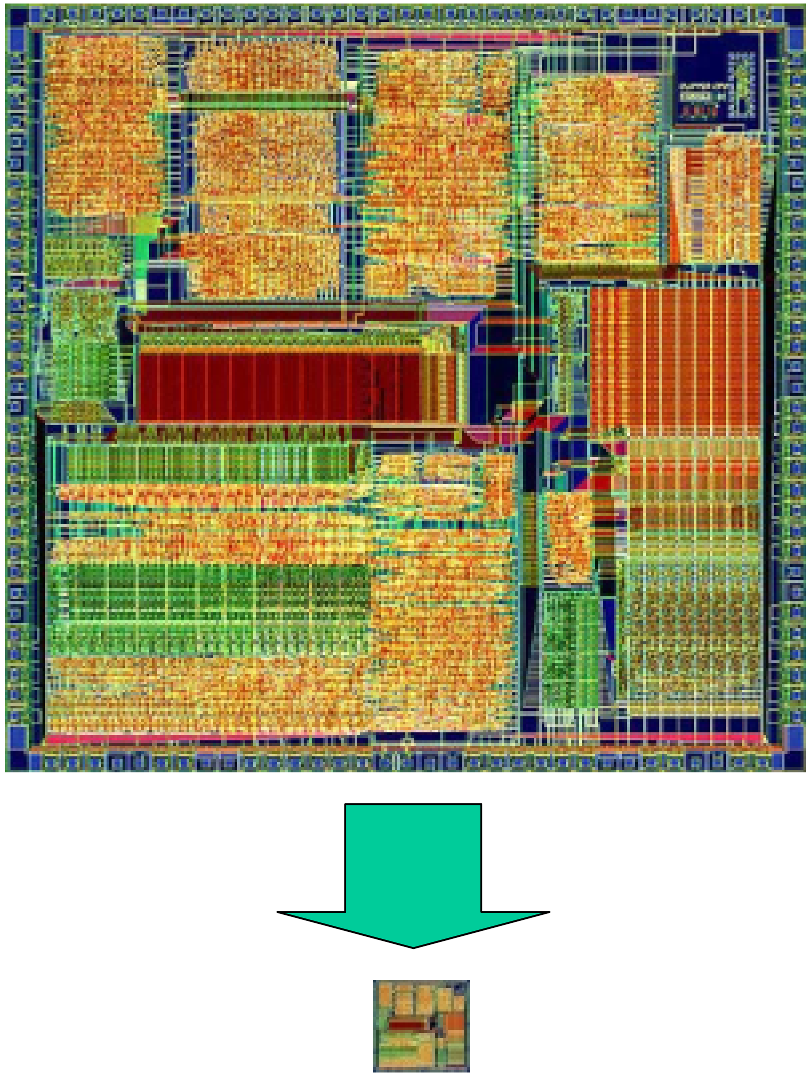
- Lg ~ (10 nm – 45nm)
- Fin width ~(<10 – 120 nm)
- Fin height: 50 nm
- Tox ~ 2.5 nm

Deep Scaling - World's Shortest Gate Length FET (18 nm) With Useful Electrical Characteristics (IEDM 1999)

The Challenge of the 20 nm Transistor Circuit

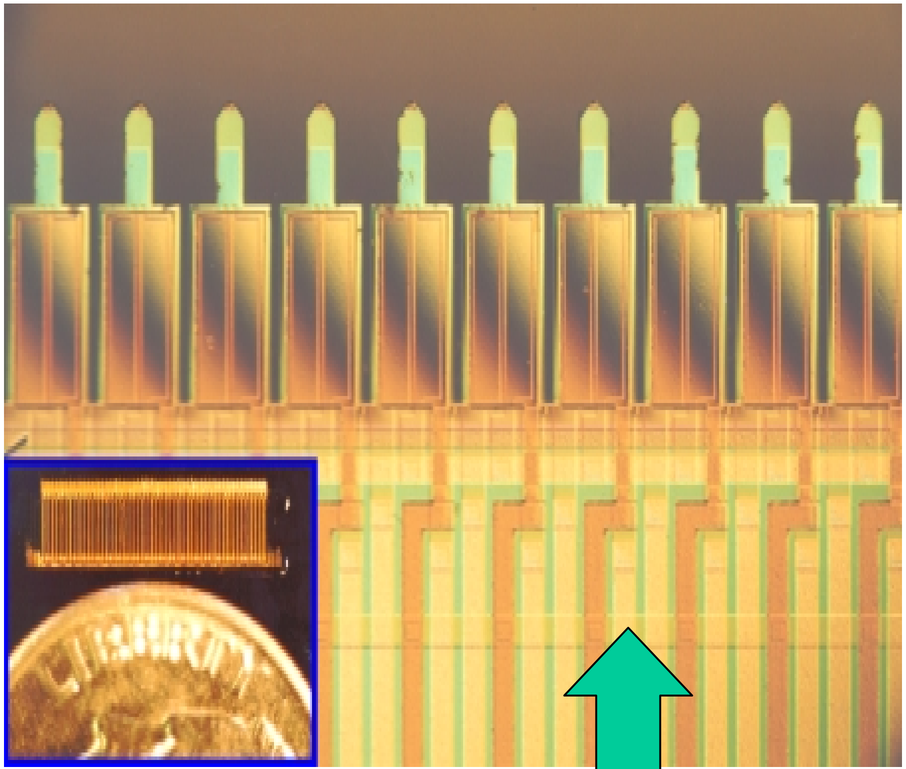
- $>10^{10}$ transistors per chip
  - Patterning
  - System design

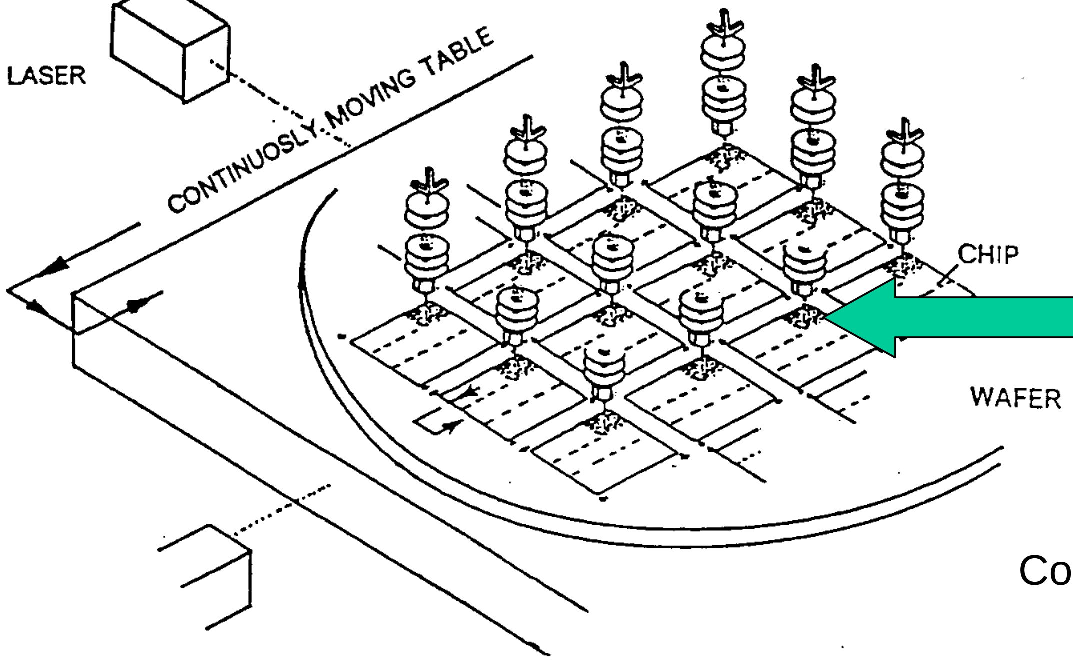




Maskless Patterning

- Low volume (~1000 wafers per mask) dominated by mask cost
- Eliminate mask!



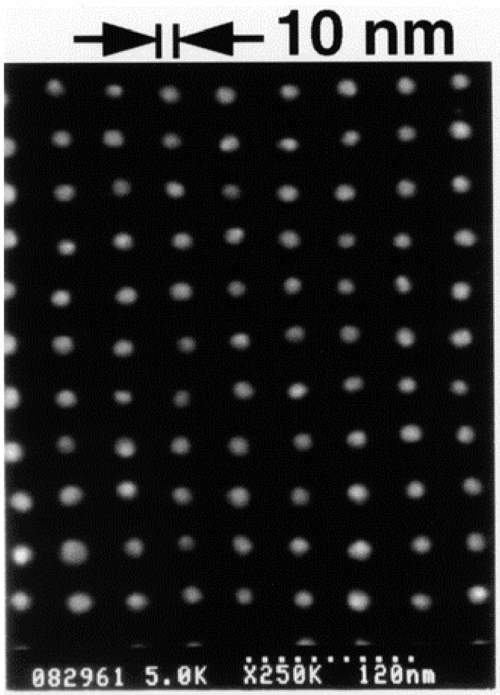


Multiple probes

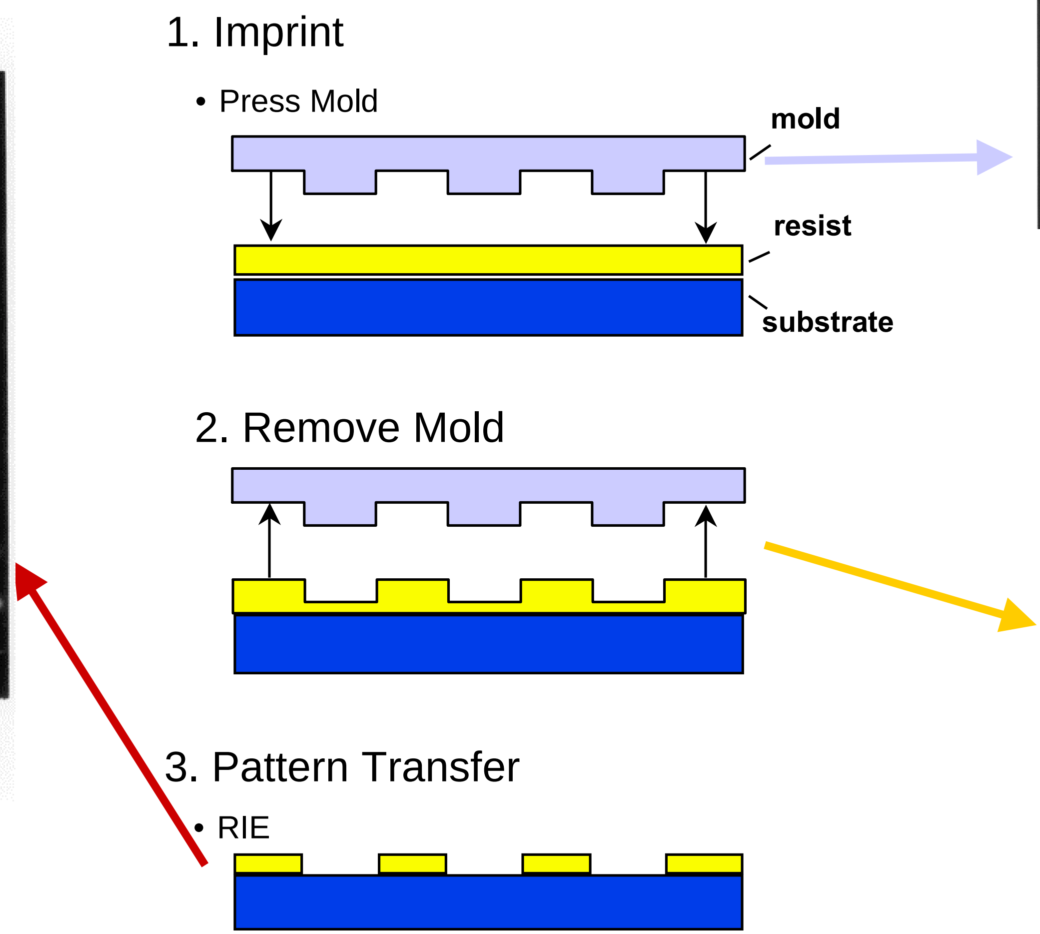
Multiple electron columns

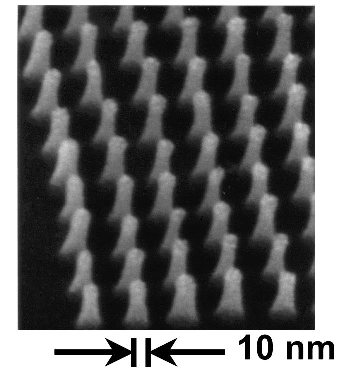
Courtesy of Stanford University and ETEC

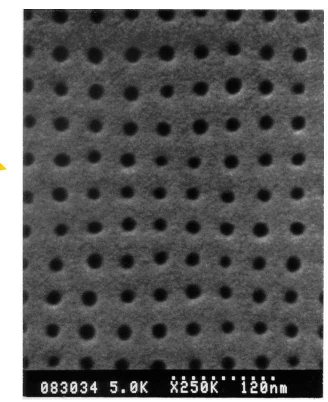
Nanoimprinting (Chou, Princeton Univ.)



10 nm Metal Dots







- Phenomenal resolution over large area
  - <10nm over several cm^2
- Wide range of ‘printing actions’
  - Patterns of self-assembling ‘ink’

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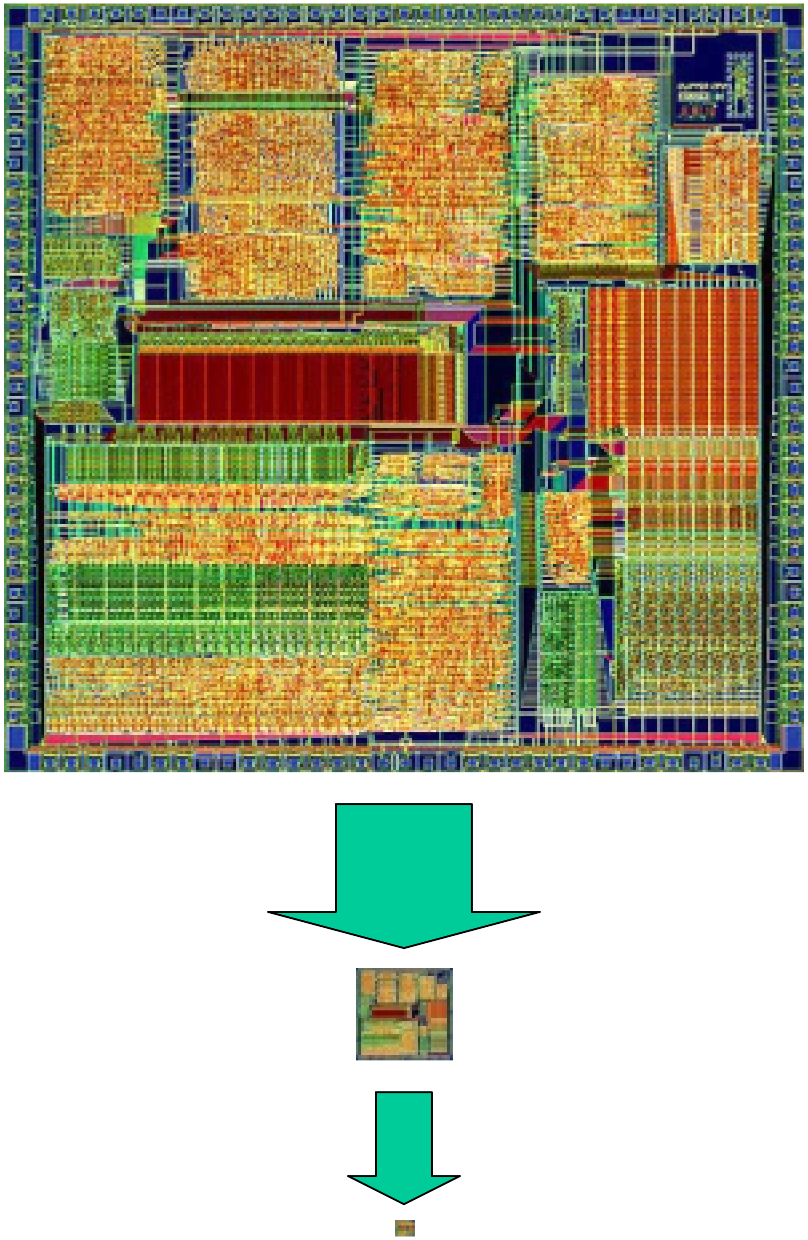
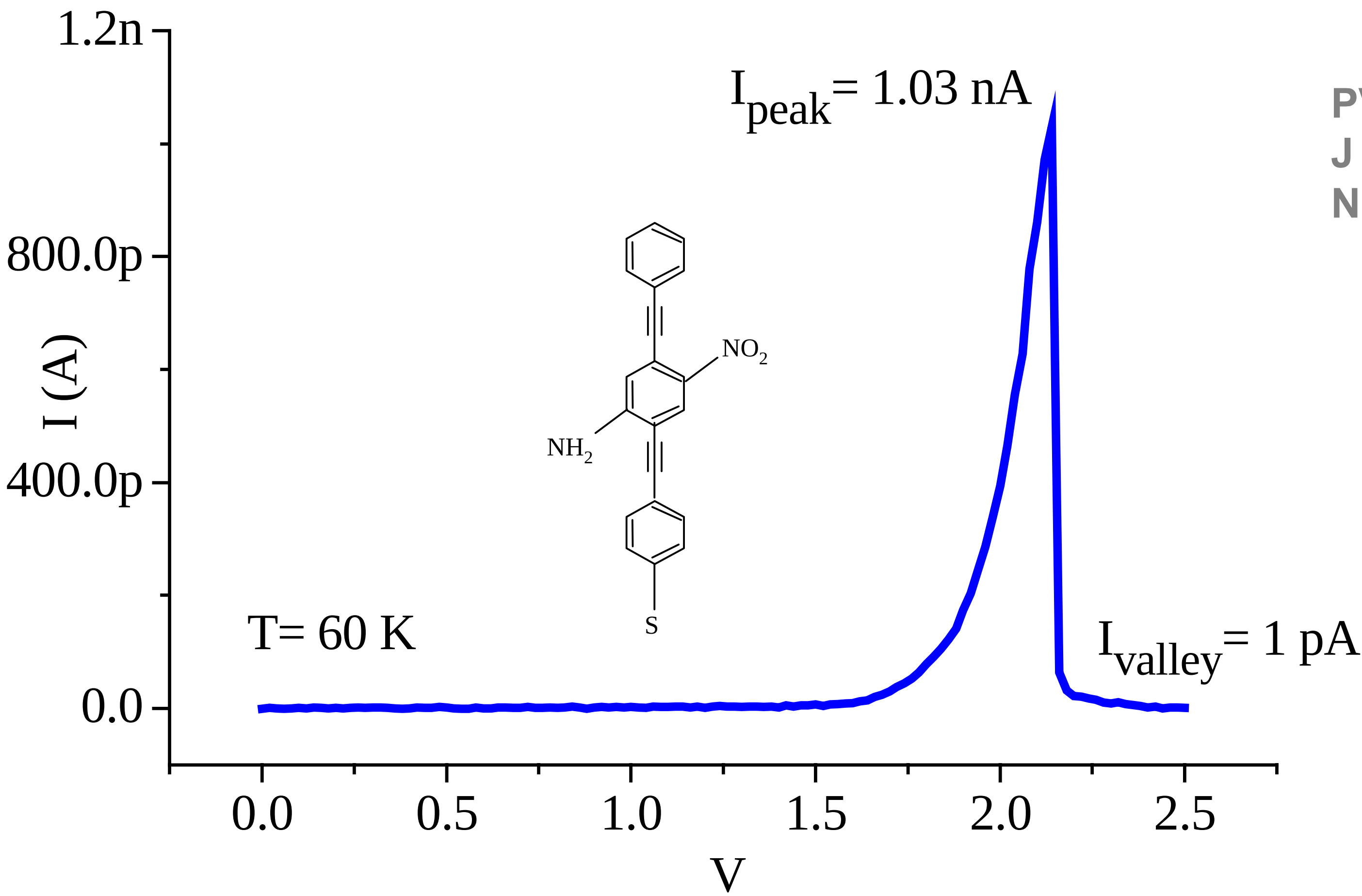
Moletronics (Molecular Electronics)

The roadmap to 10^{11} devices per chip

- Molecular based switches
- Assembly rather than fabrication
  - Defect tolerance
- Scalability



Electrical Properties of Molecular Diodes



PVR = 1030:1
J = 53 A/cm^2
NDR = -380 μΩ-cm^2

- <30nm diameter active device
  >10^{10} bits/cm^2

- Room temperature
- Reversible

Yale University, Rice University
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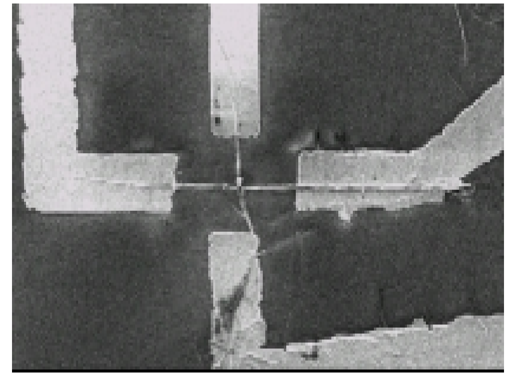
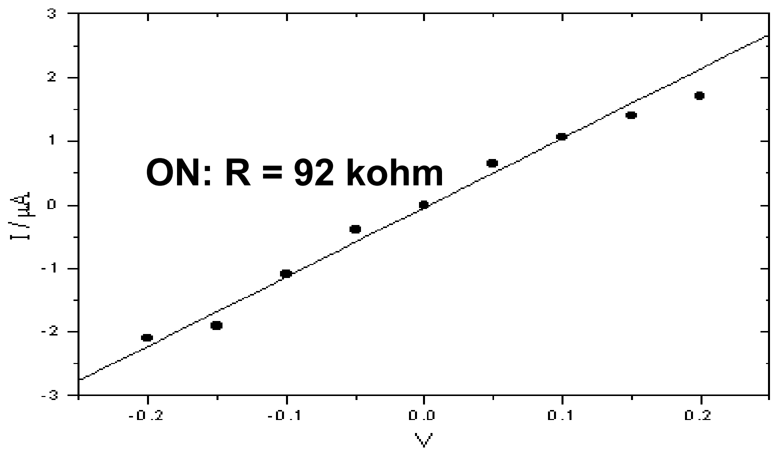
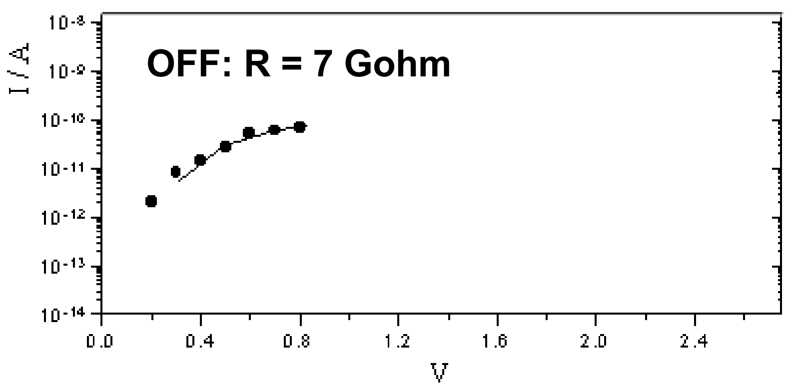
Control of electronic properties by chemistry

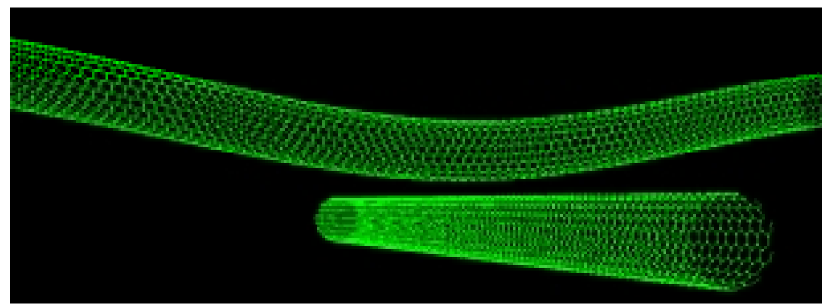
Carbon Nanotubes: <10 nm^2 memory bit

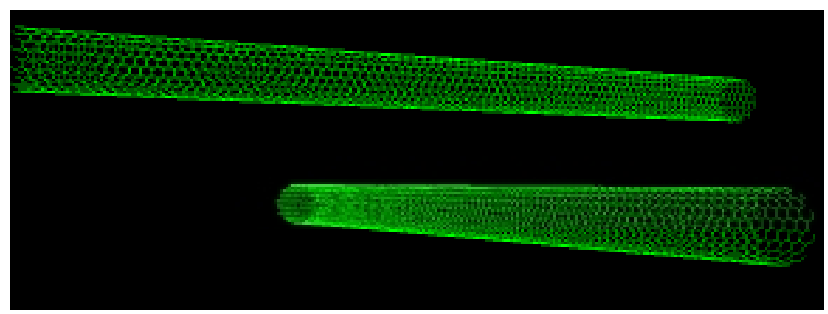
- Large on-to-off ratios (10^5:1)
- Low power: CMOS ~ 1 nW/device,
  Cross bar < 1 pW/device











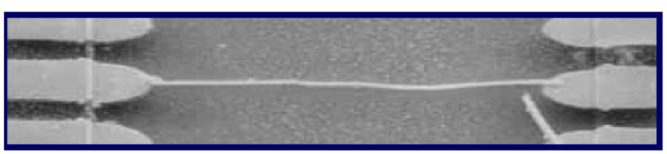
Room temperature reversible memory

Harvard University, Stanford University

Hierarchical Assembly: An alternative to slicing and dicing

- Let thermodynamics do the hard work
  - Molecules and nanowires into nano-arrays
    - Carbon nanotubes
    - Molecular self-assembly
  - Nano-arrays into micro-modules
    - Field driven alignment
  - Input and output
    - Fluidic assembly

Chained 200 nm Au wires



E-field Assembly,
Penn State

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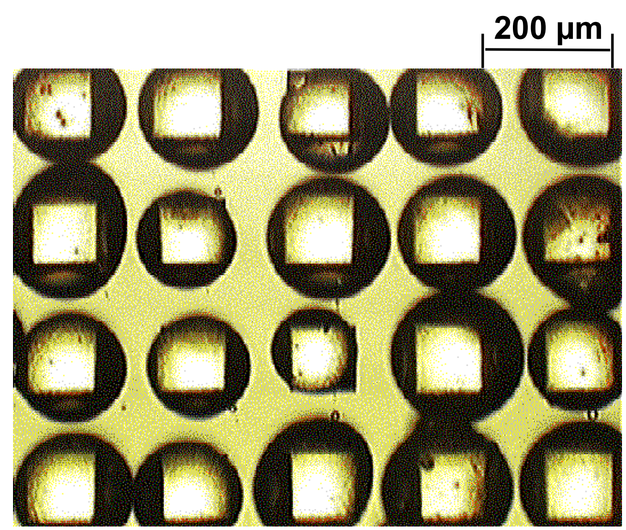
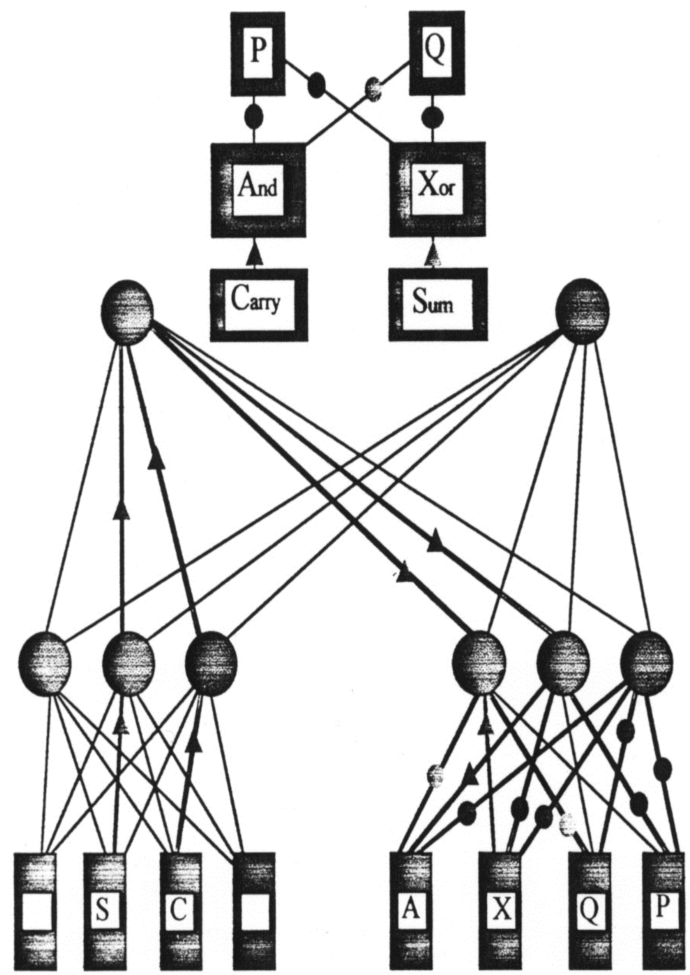


Fluidic assembly of
arrays of spheres, HRL

Scalability

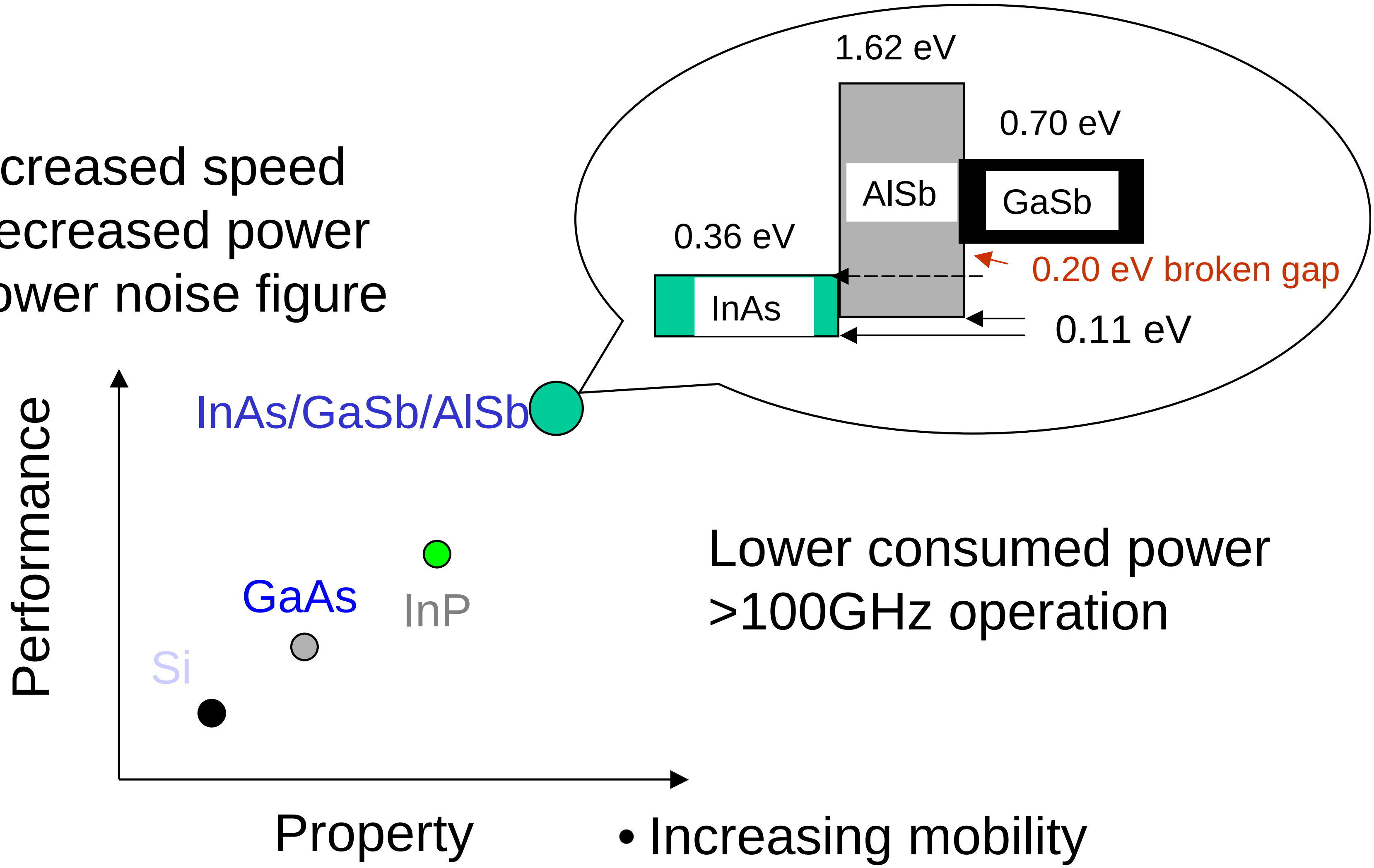
- Scaled CMOS   Gigascale systems on a chip
- Moletronics has the potential of tera (not terror) scale integration
  - 10^{12} devices
- Need systems architectures to be scalable to these levels
  - Defect tolerance
  - Programmability
  - Access times
- Hard challenges but enormous pay-off



UCLA/HP: Fat Tree Architecture

Nanoelectronics: New Materials

- Increased speed
- Decreased power
- Lower noise figure

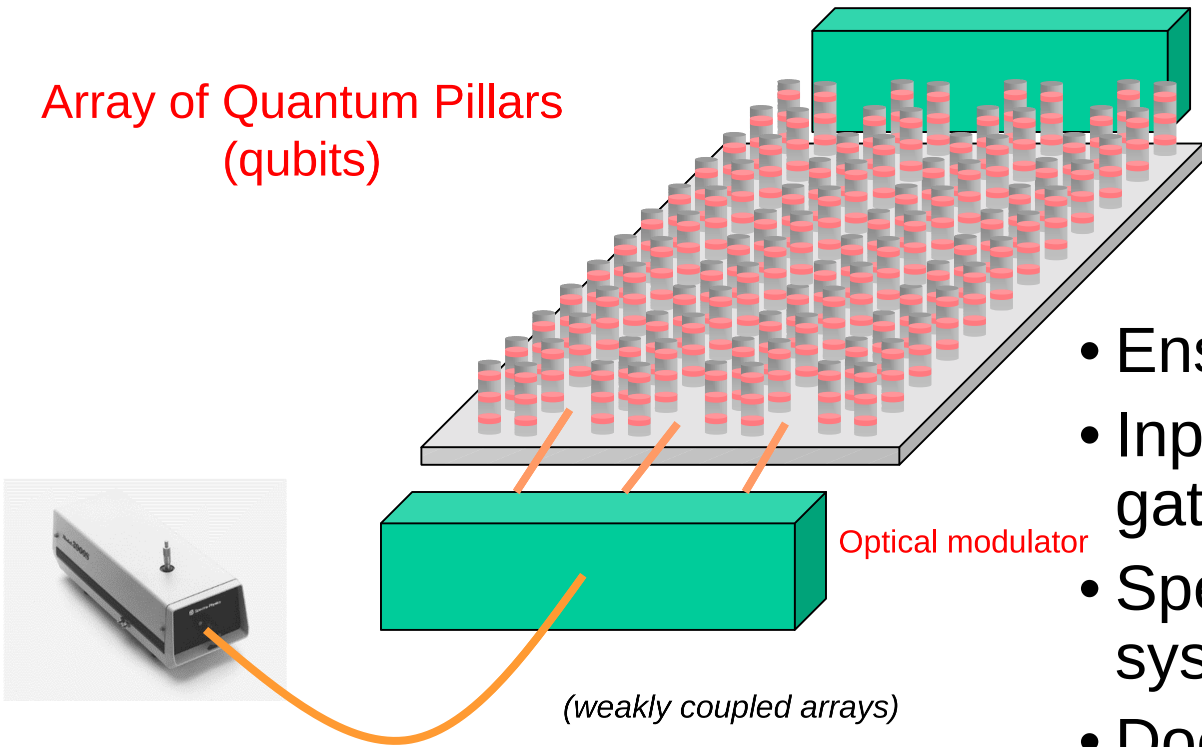


Lower consumed power
>100GHz operation

- Increasing mobility
- Decreasing bandgap
- Increasing lattice constant
- Decreasing effective mass

Nanoelectronics: New Challenges

Scalable Quantum Computing



- Ensemble of devices/qubits
- Input signal acts as a logic gate
- Spectroscopy to read system output
- Does not require connectivity or coupling between adjacent devices

The Future

- Incredible opportunities and challenges exist
  - Multi-functional electronics systems combining the best attributes of inorganic and organic materials

- We aren’t done yet!