3D Microsystems

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Outline

- 3D Silicon Systems
- Polylithic Technologies
  - Heteroepitaxial growth
  - Layer transfer and bonding
  - Fluidic assembly of III/V chiplets on Si
  - Miniature mechanical filters
- Future Directions

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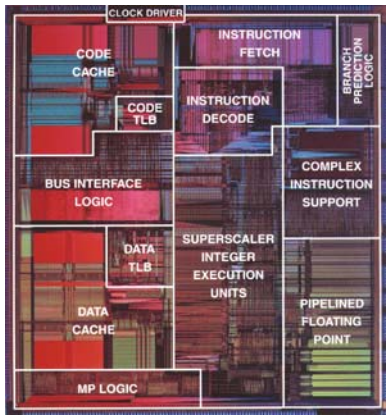
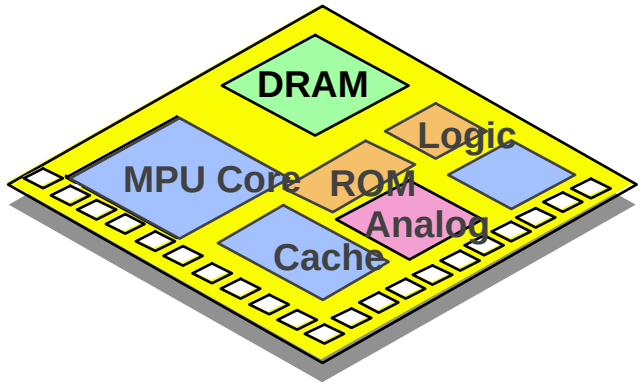
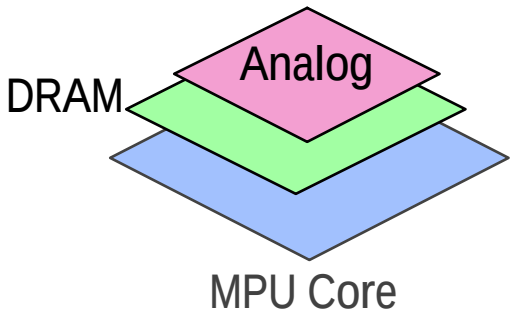
The Debate

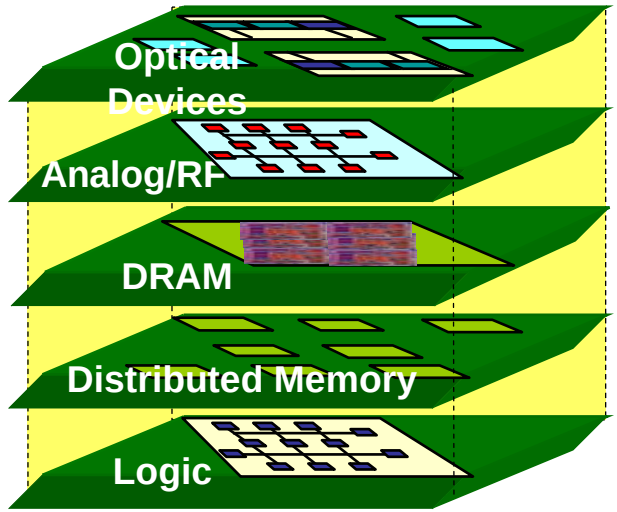


System on Chip





System in Pkg, SiP



3D IC

3D IC

What exactly is 3D? How many layers is right?

Technologies? Wafers, chips, true 3D, or permutations?

Applications, Performance, and time to $

The practical: Thermal, mechanical electrical, yield

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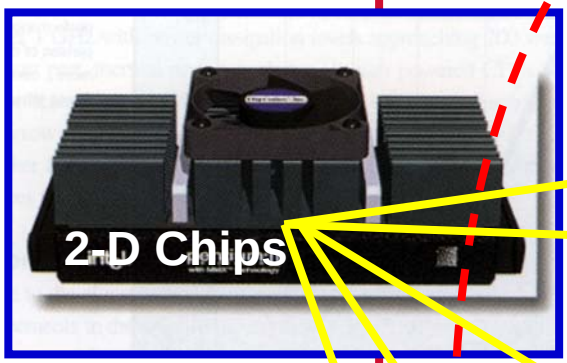
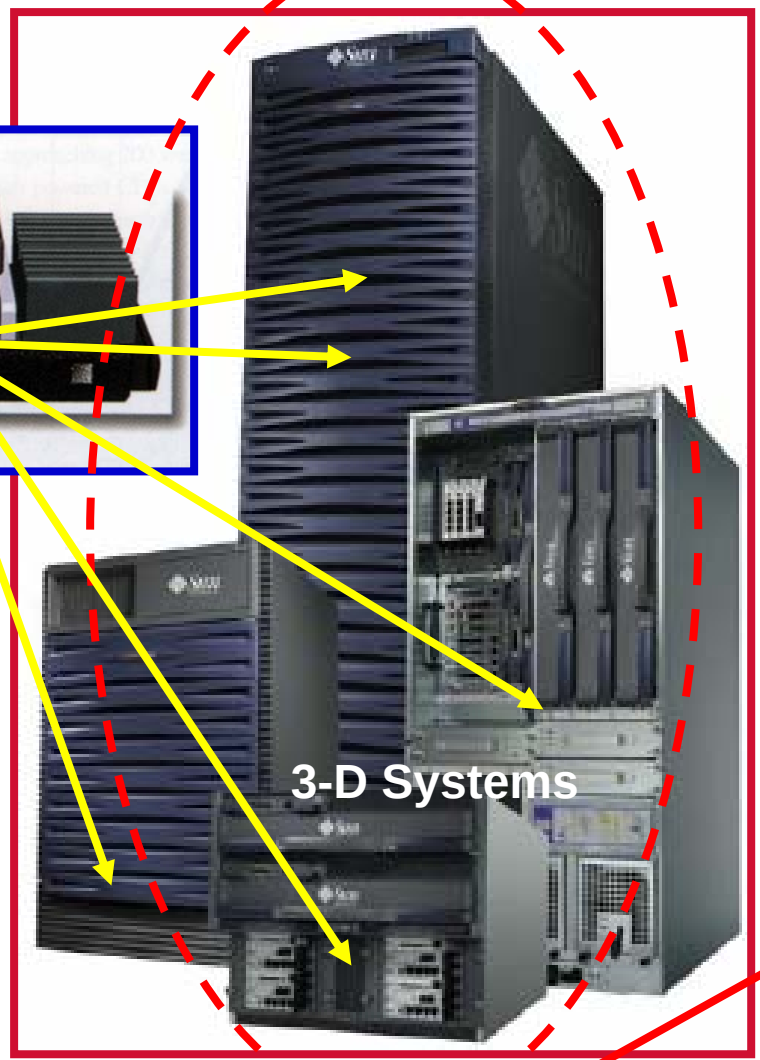
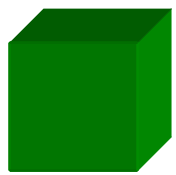
The Bottom Line





What are the systems that will be built from 3-D Chips?



3-D Chips/Microsystems

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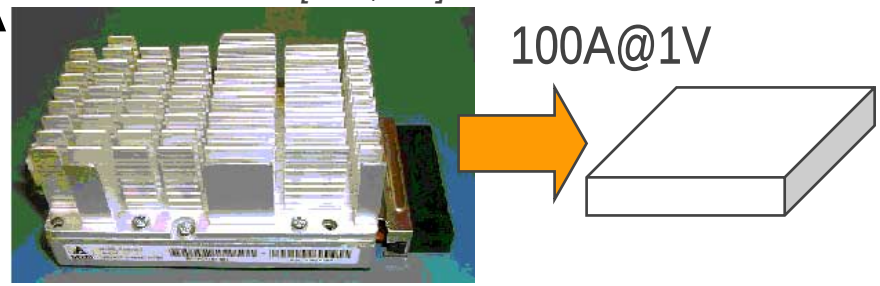
3D Integration and Power Management

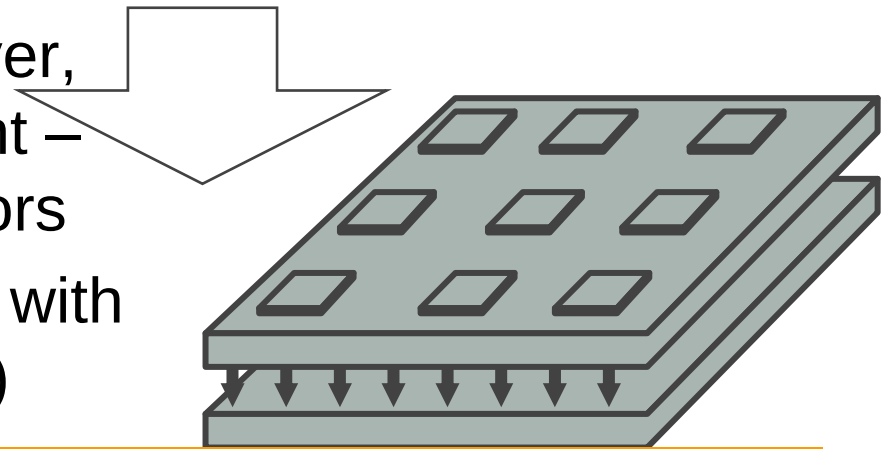
Get the power in

- Processor power supplies around 100W at 1V => 100A
  - R=1mΩ implies 100mV drop
- Problems: current density, di/dt, power rail self heating

[Intel,2002]



- Distribute 48V to power layer, only 2A input supply current – using high voltage transistors
- Area-distributed regulators with high-quality passives (L, C)



3D Integration allows inherent insertion of power management functionality

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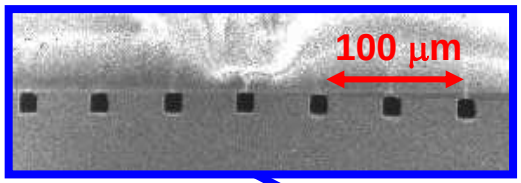
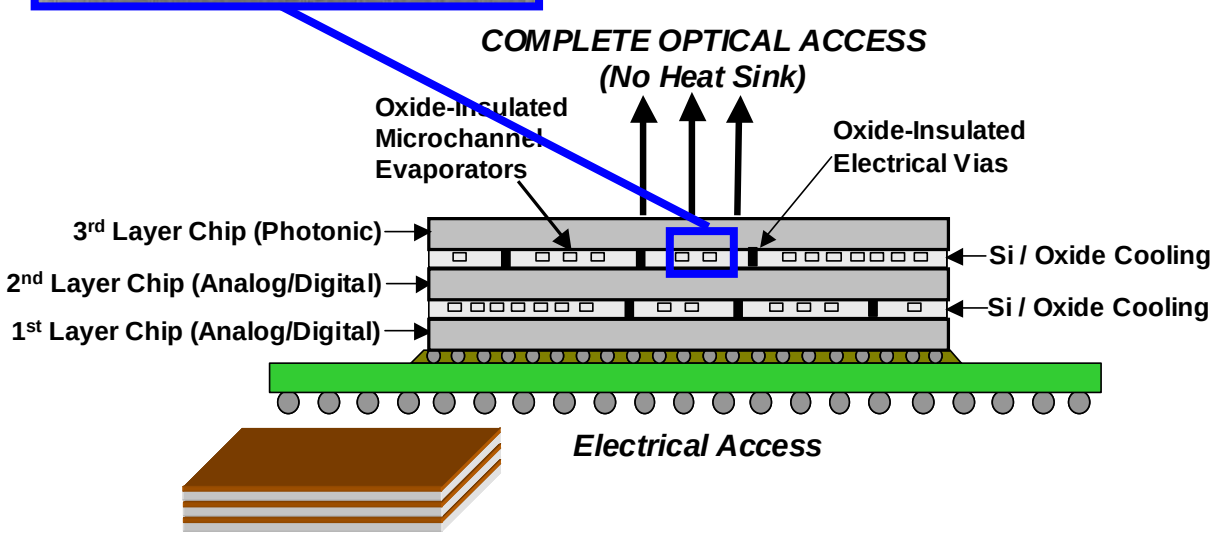
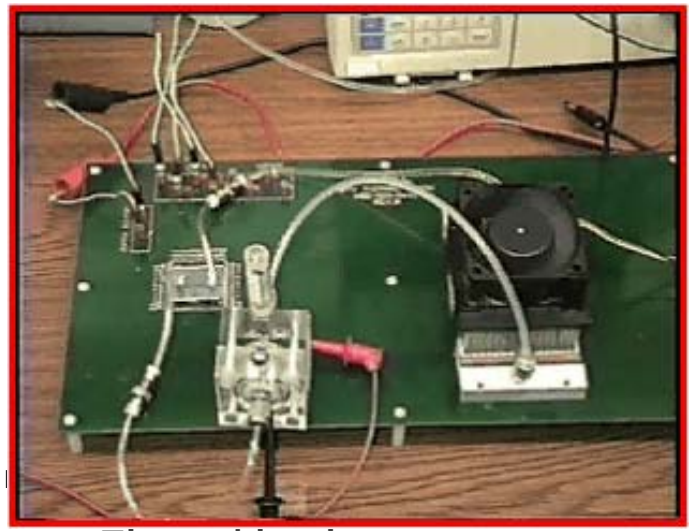
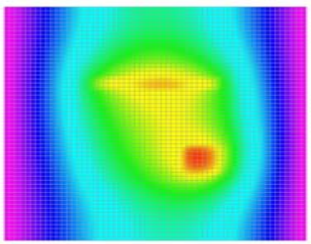
Microchannels Get the Heat Out

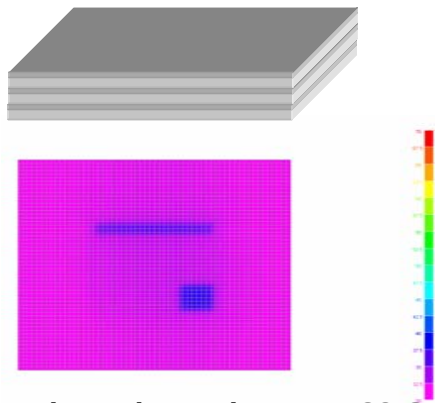






Electrokinetic pumps
No moving parts
5W for 200W cooled





Cu heat spreader Tmax: 69 C

Micro channel Tmax: 39 C

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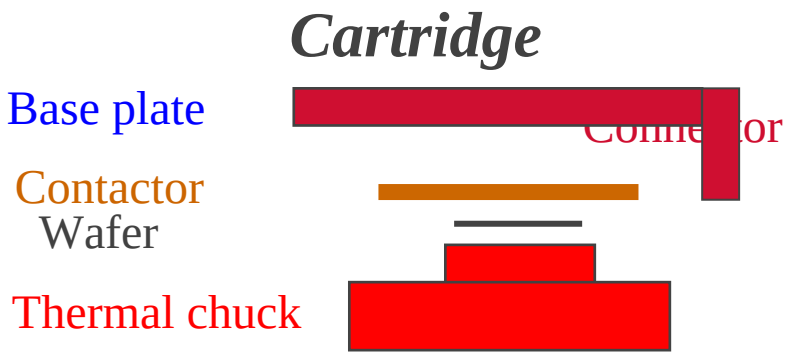
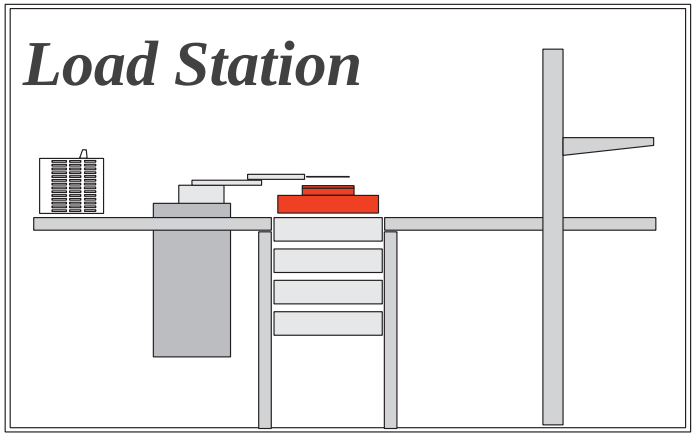
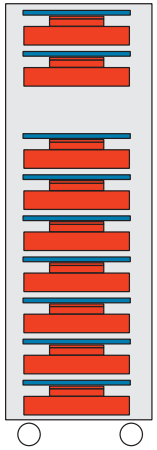
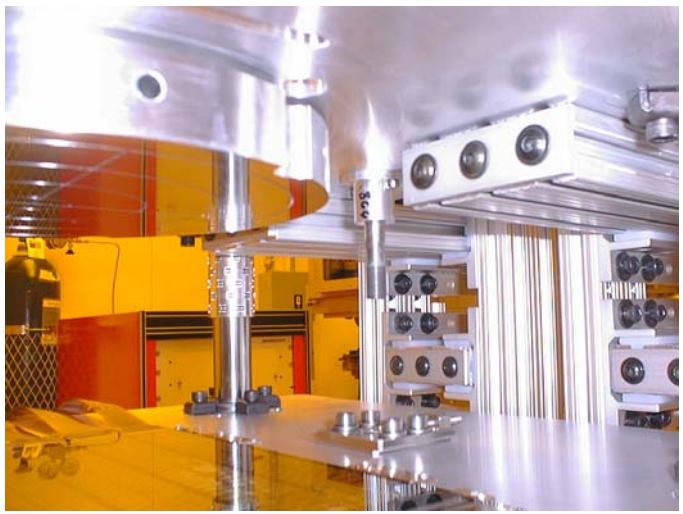
Wafer Level Burn-In and Test Capability

Aehr Test



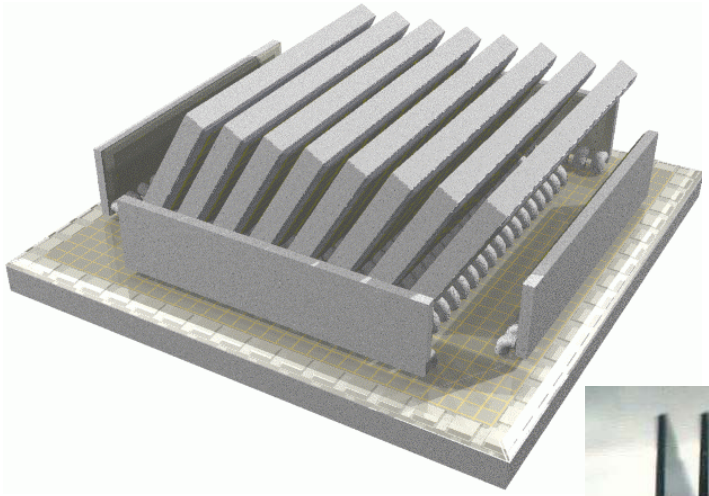


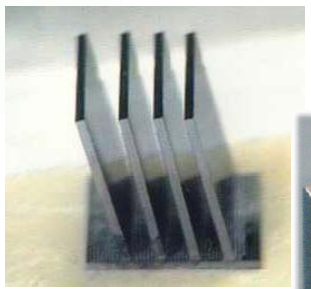


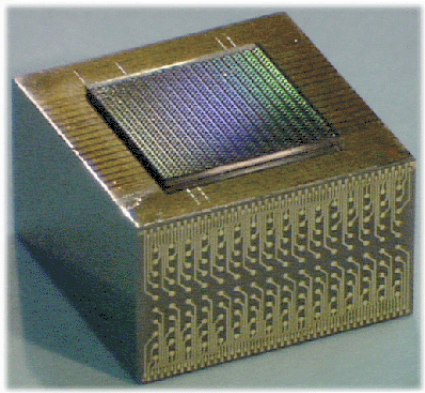


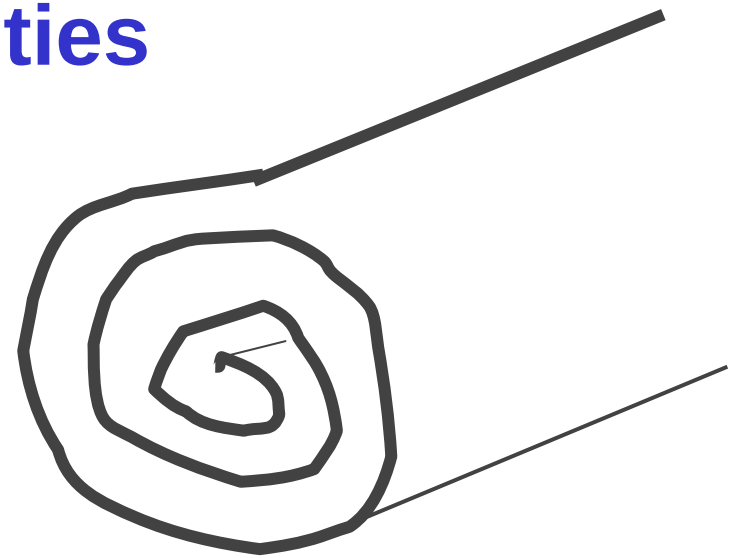
Excellent temperature uniformity and full wafer contact established

Other 3-D IC Possibilities









Processor+Cache

FPA on Stacked ROIC's

- Massive Memory
- Compact Wafer Scale Systems
- Fold-out Structures (RF)

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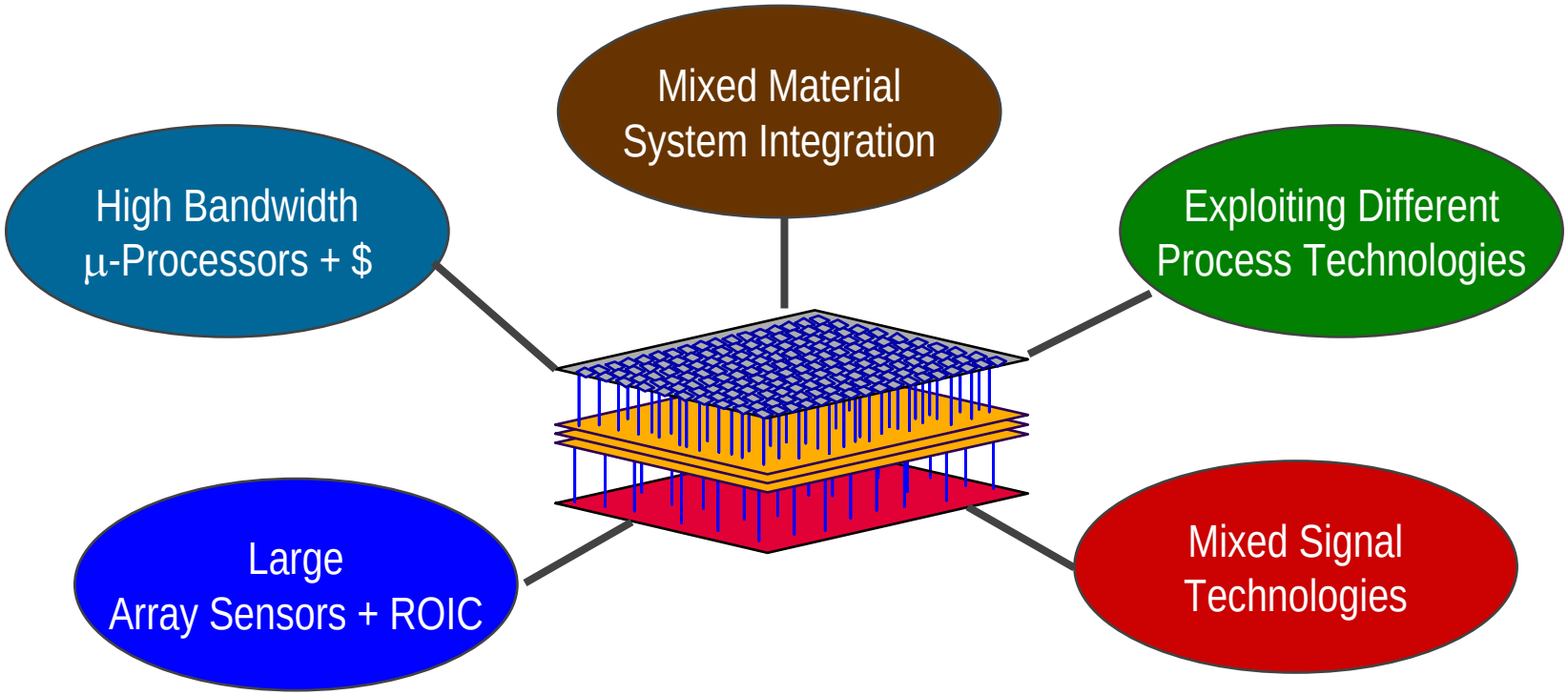
3-D Circuits – The Big Space



3-D Offers More Transistors Per Unit Volume Than 2-D, And a Platform for Integrating Other Technologies and Devices (MEMS/Opto/Compound Semi./Materials/etc.) to Build Low Power, High Performance Microsystems….

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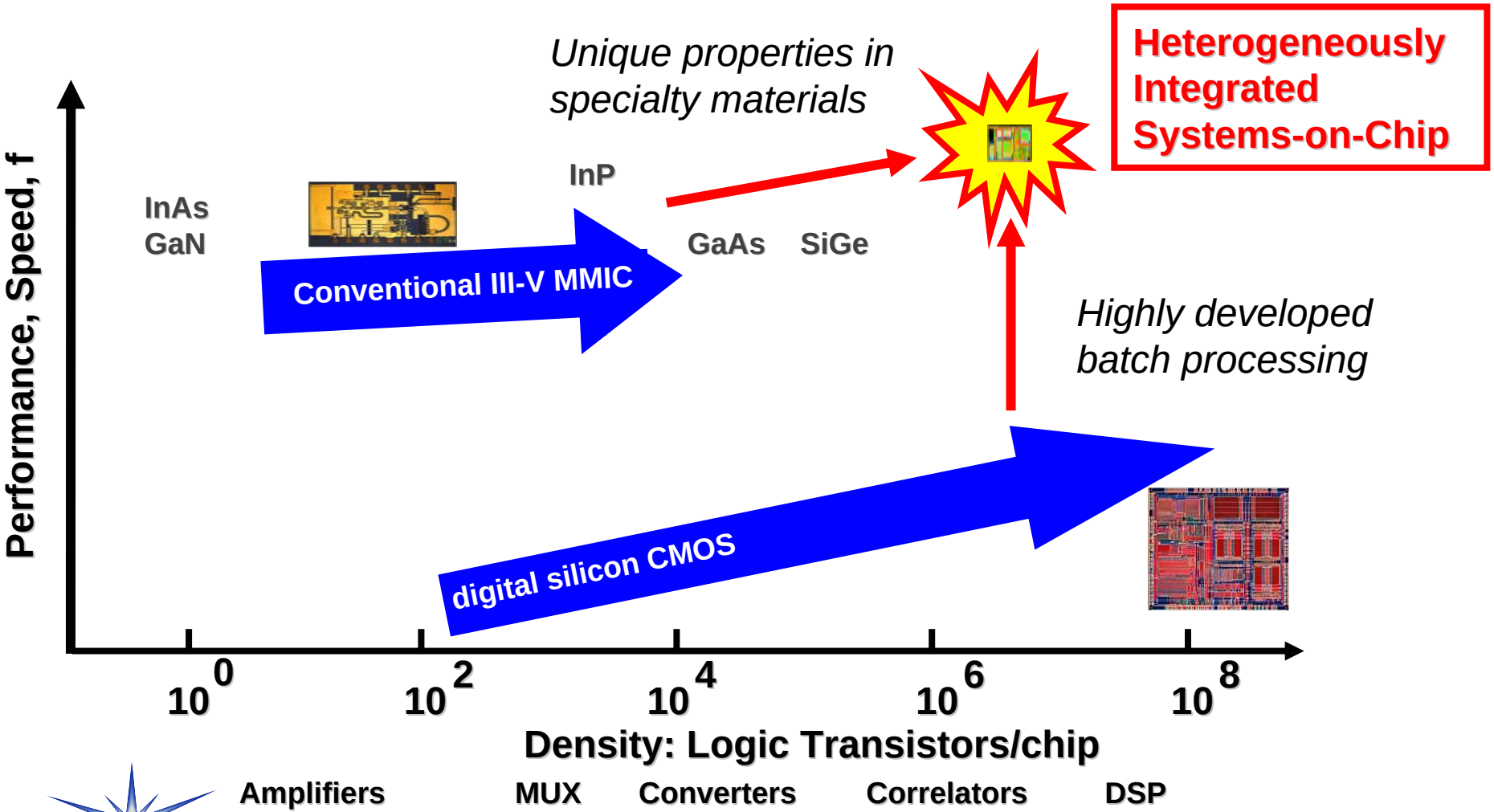
Chip Performance Space



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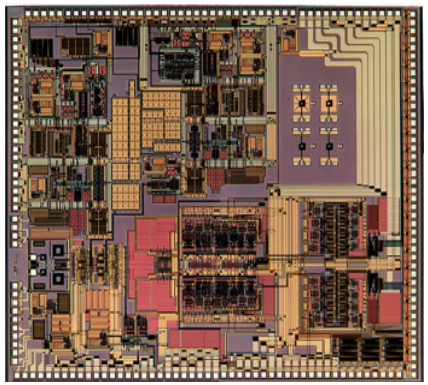
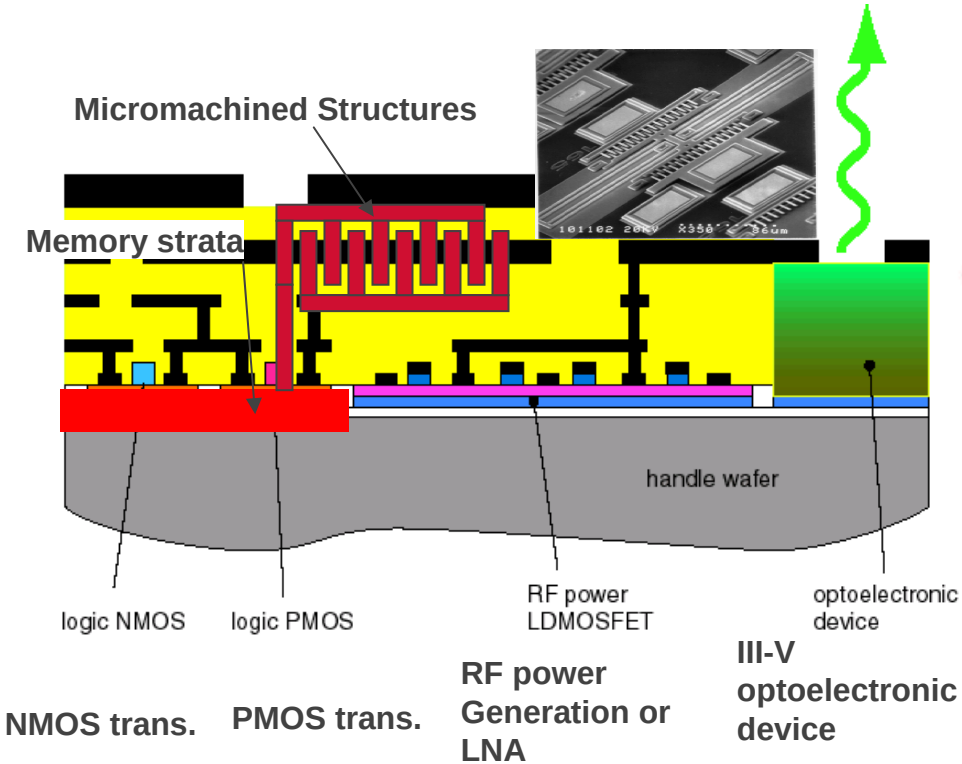
Polylithic Integration…..

Incorporating the best technology for each function





Direct Fabrication for: Systems with the greatest possible RF bandwidth and dynamic range, Reduction in power and improvement in thermal, Tight coupling to sensing/actuation

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A Working Definition

- Polylithic Integration = More than 2 disparate materials or technologies integrated in a single fabrication sequence.
  - One to billions of useful devices per material
  - Parallel process for forming connections useful but not required
  - Not necessarily based on silicon

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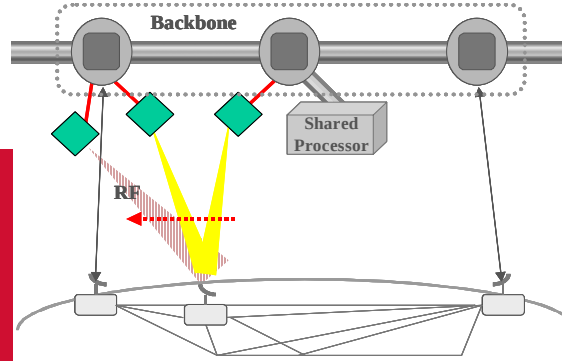
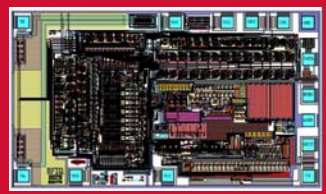
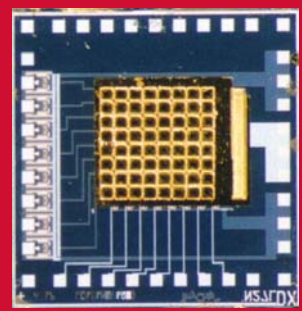
Some Applications…

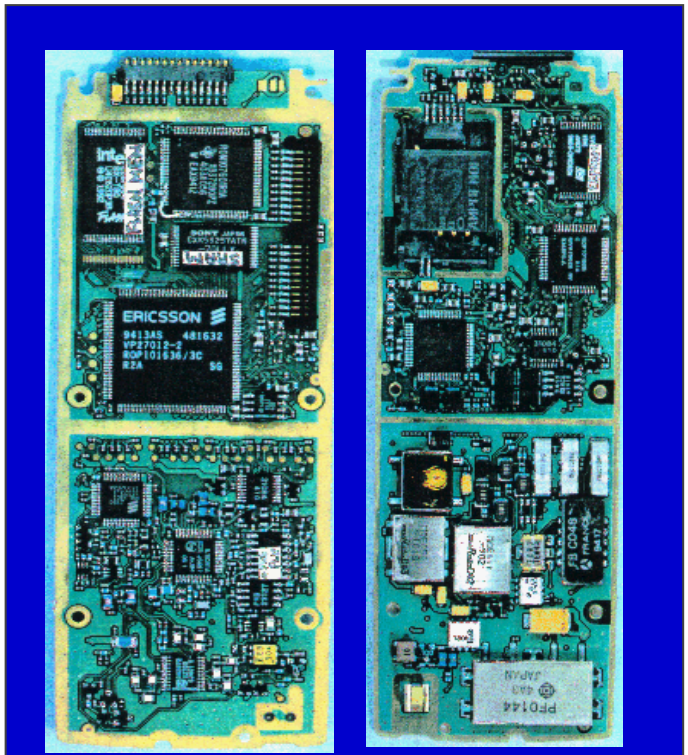




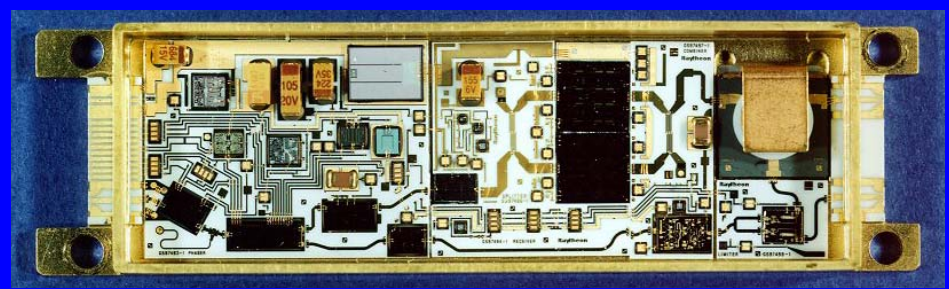
Ubiquitous Sensor Network



Focal Plane Arrays



III-V+Si+Passives Integration



T/R Module

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Polylithic Integration = Heterogeneous Integration

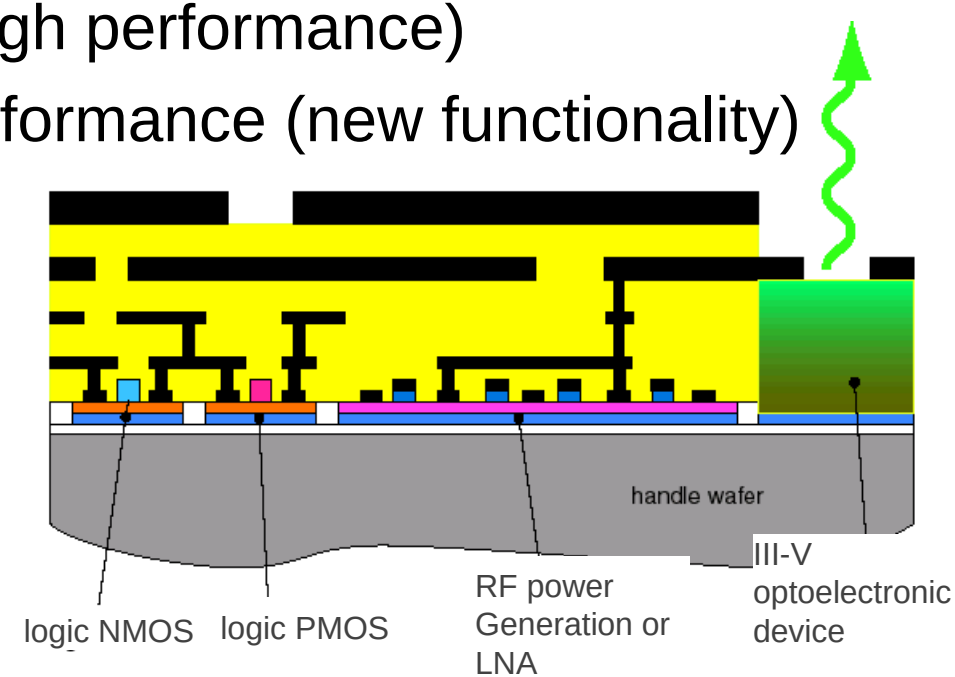
- Technologies to create microsystems that incorporate circuits/devices in dissimilar materials (the best junction for the function)
  - Eliminates lossy off-chip interconnects and need for strict 50 Ohm matching (low power)
  - Reduces latency (high performance)
  - Expands overall performance (new functionality)

HGI Technologies:

Direct Growth

Bonding

Fluidic Self Assembly



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Integrating WBG Materials With (on) Silicon

Demonstrated Process for Growing GaN on Si Wafers at NCSU, Commercialized by Nitronex for Low Cost GaN Substrates (Nitronex part of MTO SUVOS Pgm.)

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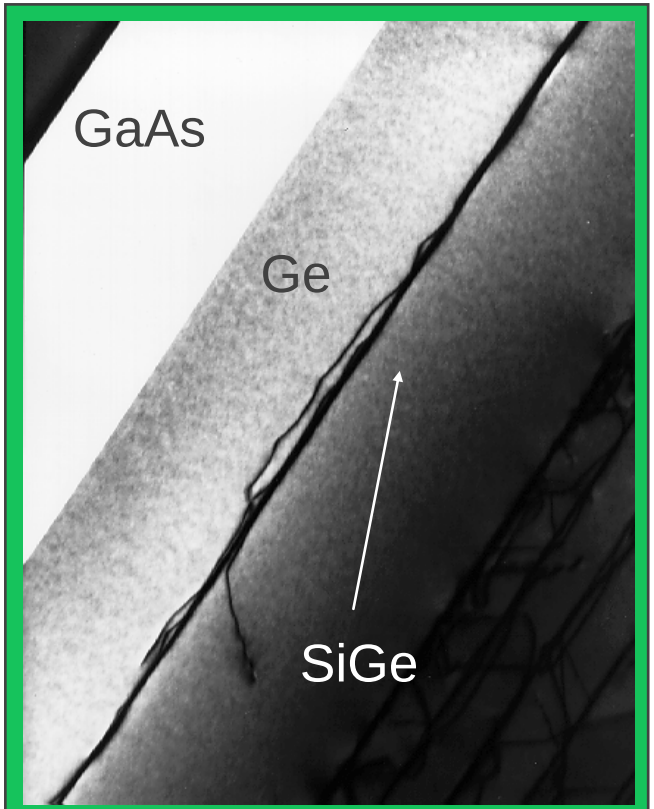
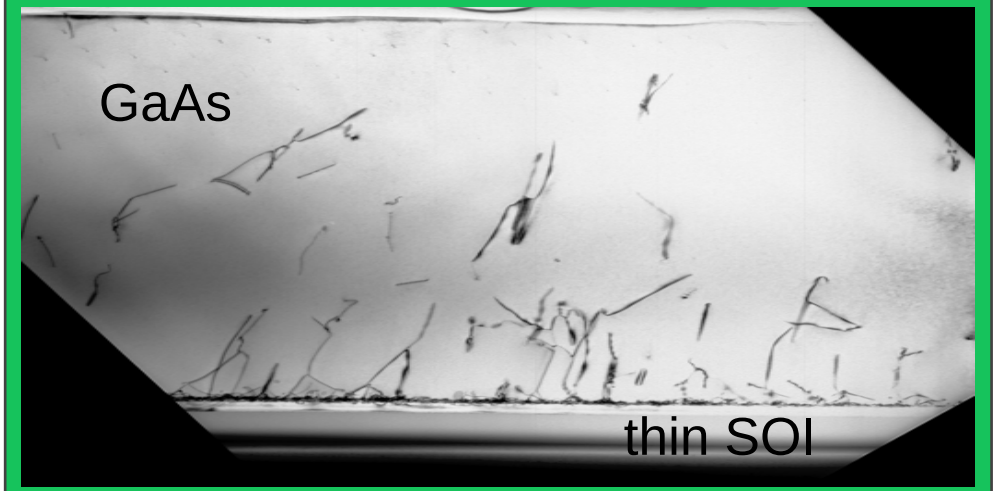
HGI Materials: GaAs on Silicon



via SiGe Graded Buffer
MIT/Amberwave



via thin silicon-on-insulator as compliant material Columbia University/Lucent

Achieved:

- lowest defect density ever reported (1E6/cm^2)
- long minority carrier lifetimes (10ns)
- low threading defects (<fewE5/cm^2)

Grown GaAs on Si Now Ready for Device Processing

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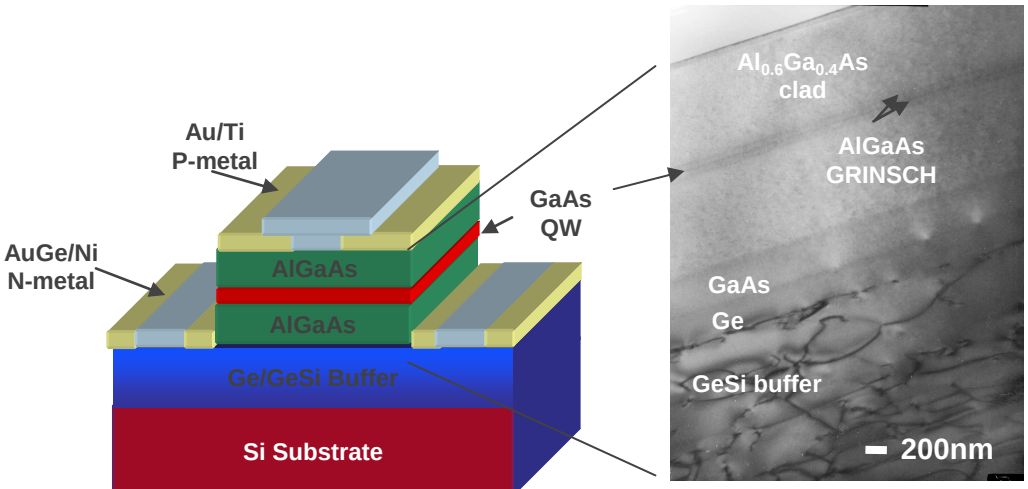
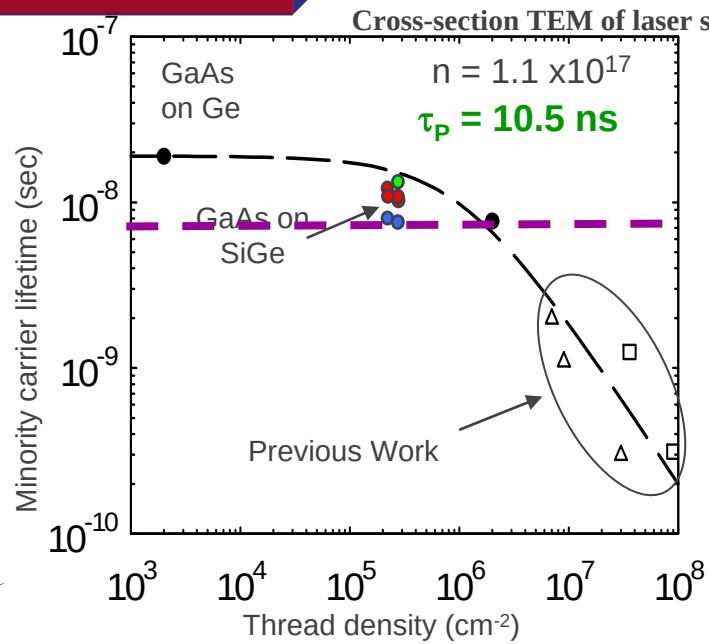
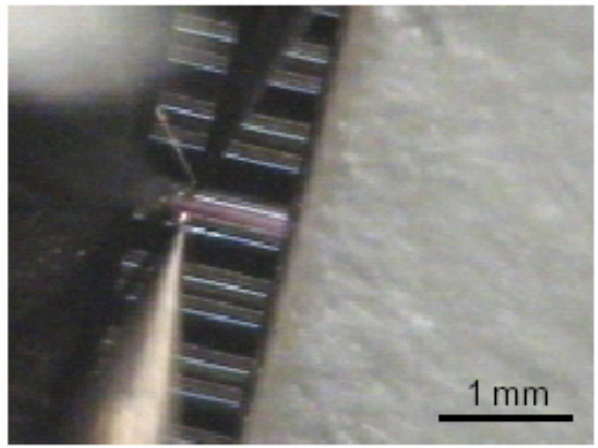
III-V on Silicon Optical Devices Function!



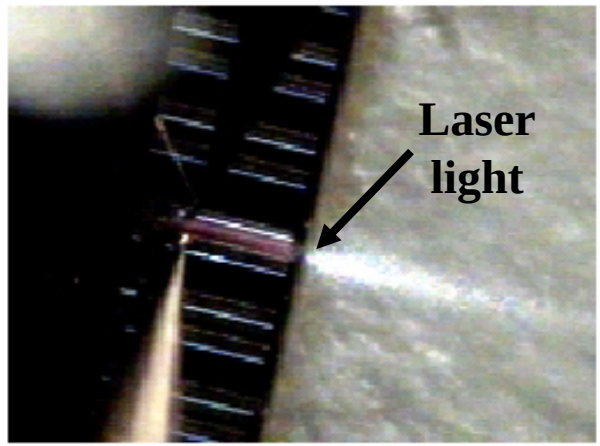
Cross-section TEM of laser structure on Si



GaAs/AlGaAs QW laser on Ge/GeSi/Si

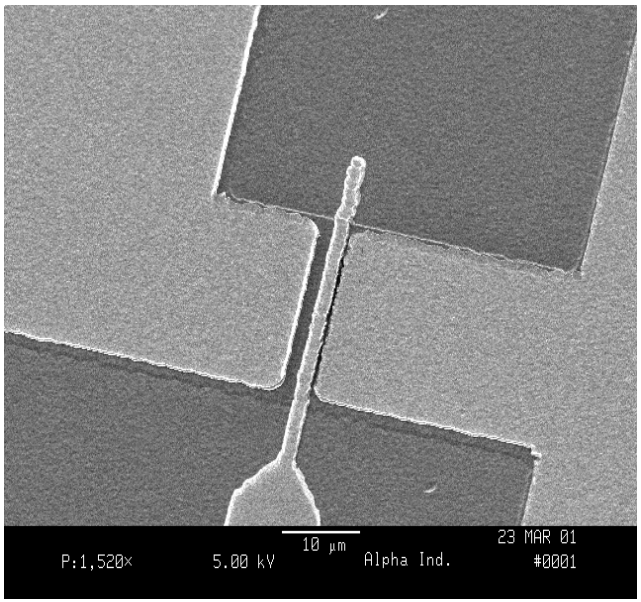


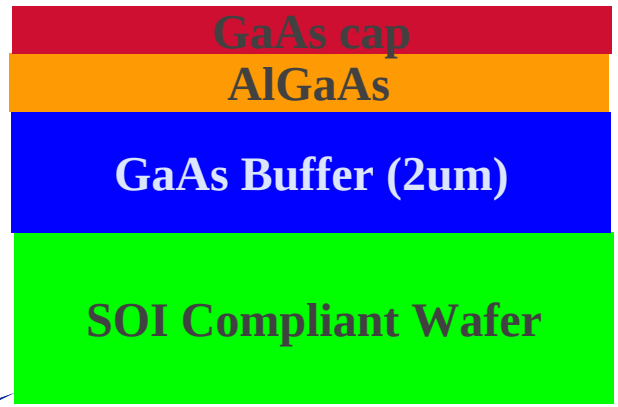
Below threshold

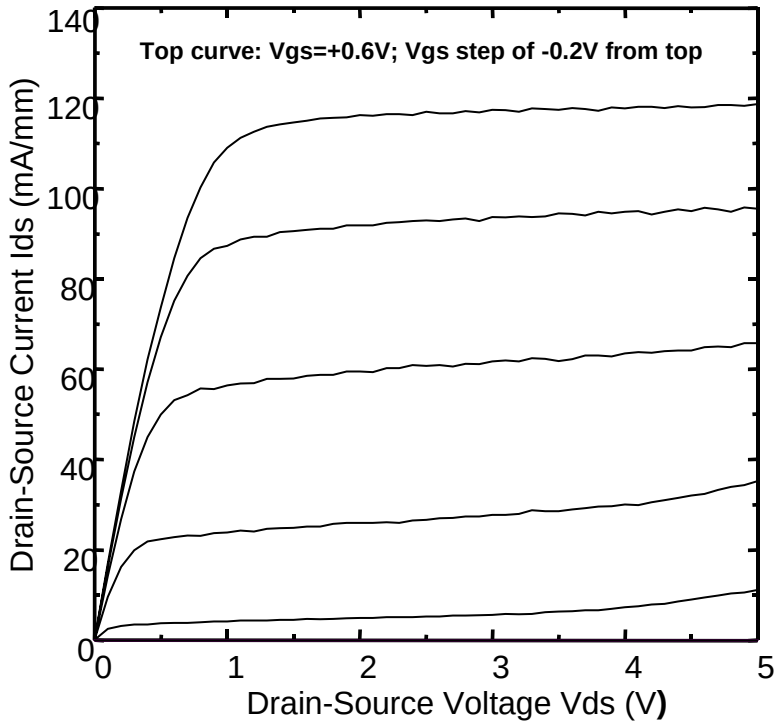


Above threshold

AlGaAs/GaAs HEMT on Silicon (SOI)







Columbia/UCLA – Stormer/Wang/Chang

Direct Growth

+ Precision alignment possible

- Processing temperatures high
- Process integration difficult for HGI on active silicon
- Limited material set due to compatibility and lattice stress/strain

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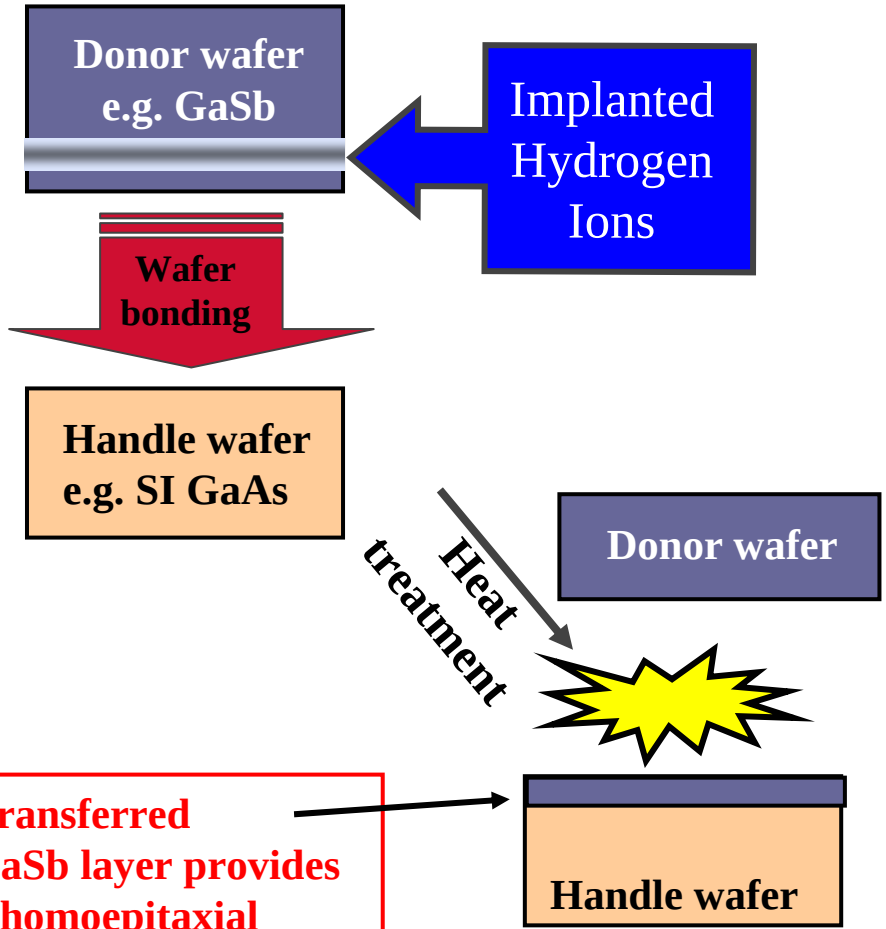
HGI: Delamination and Bonding

Ion-cut: Hydrogen induced wafer layer cleavage



Transferred GaSb layer provides a homoepitaxial substrate for device fabrication

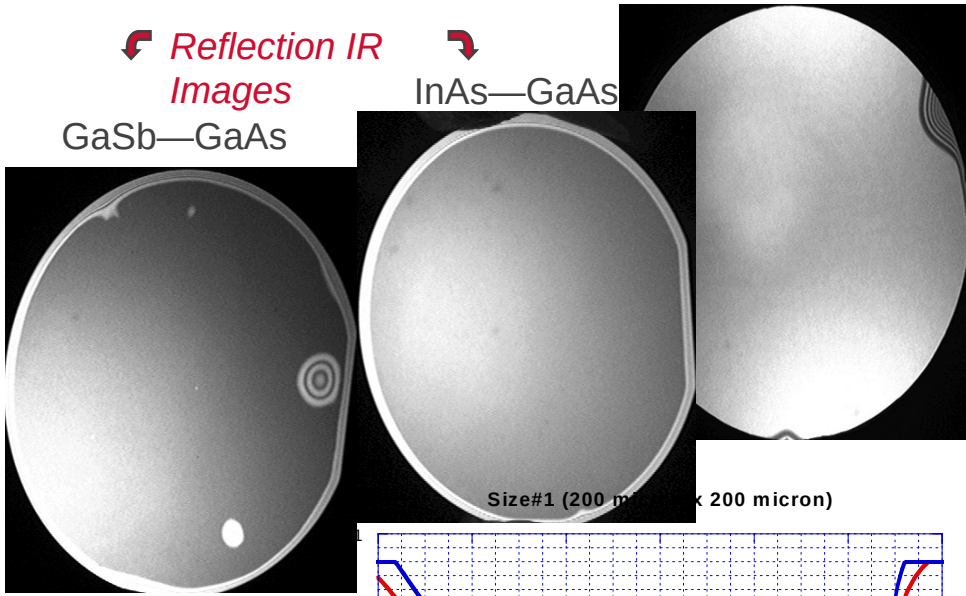
U Wisconsin

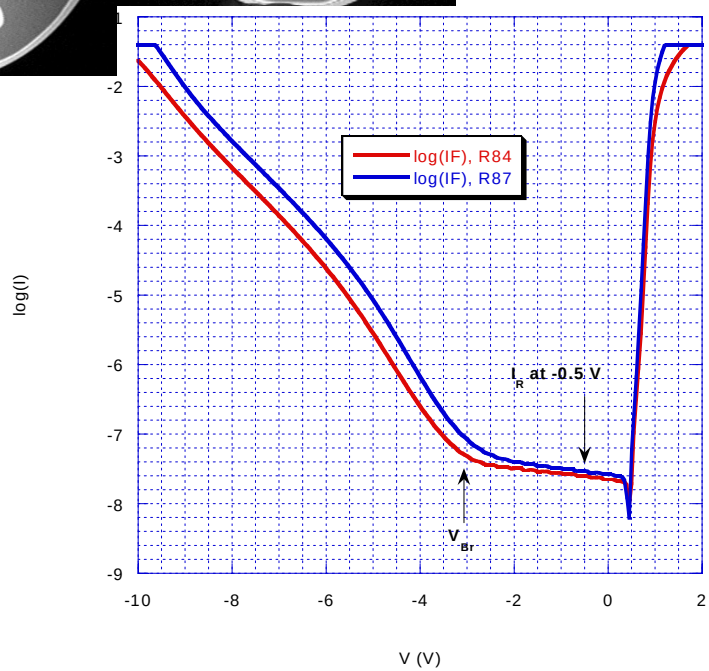
Reflection IR Images

GaSb—GaAs

InAs—GaAs

GaAs-GaAs





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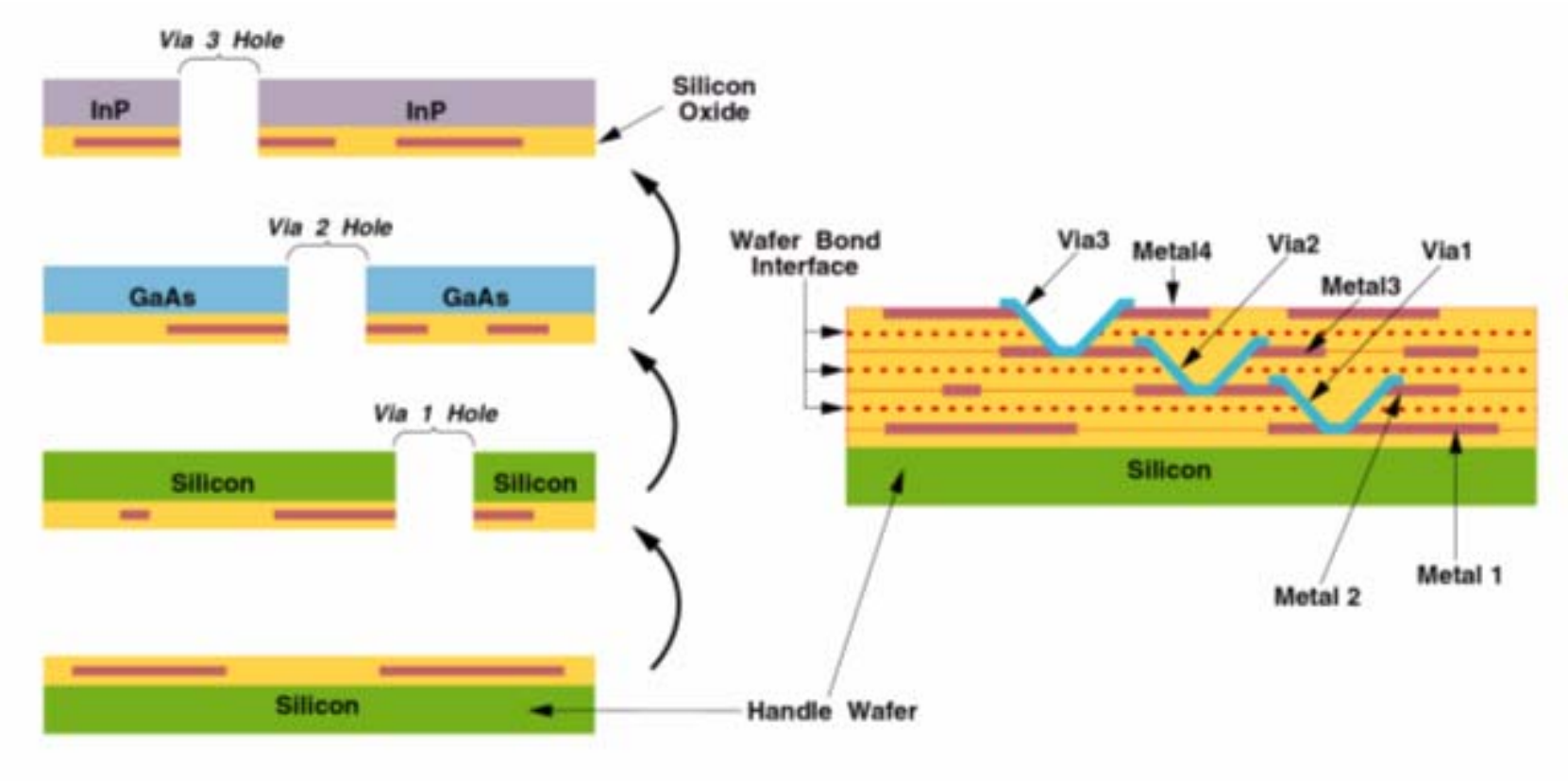
Bonding of Dissimilar Semiconductor Layers – DARPA/Ziptronix/Mayo Experimental Series



Interconnect Test Circuits

Active Test Circuits

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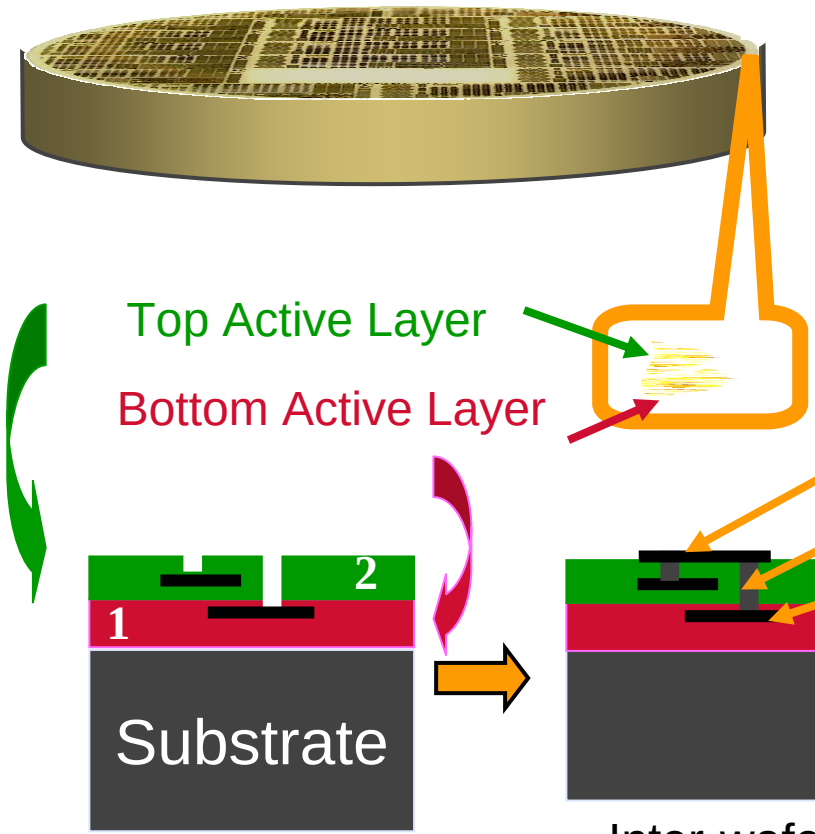
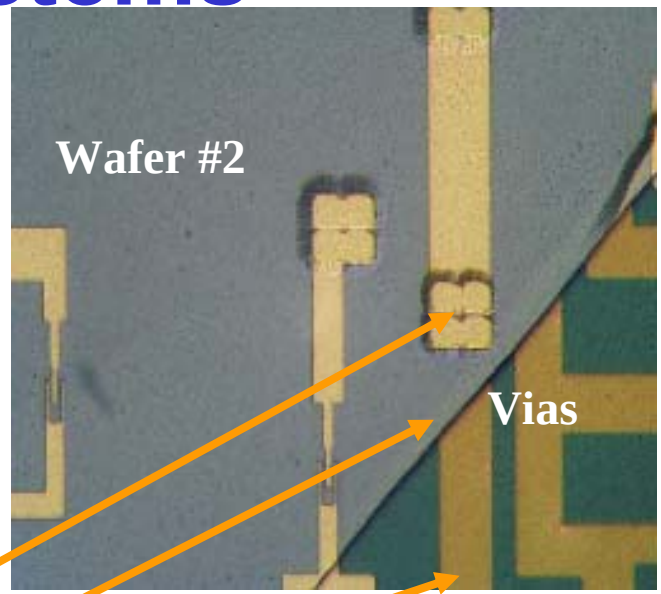
HGI: Microsystems

RTI/Ziptronix





- Planarize wafer #1 surface & pattern interconnects
- Wafer bond planarized wafer #2
- Remove 2nd wafer substrate
- Form vias through thinned wafer #2 to wafer #1 interconnect
- Deposit inter-wafer interconnect metal

Incorporate Best Device and Material for the Function

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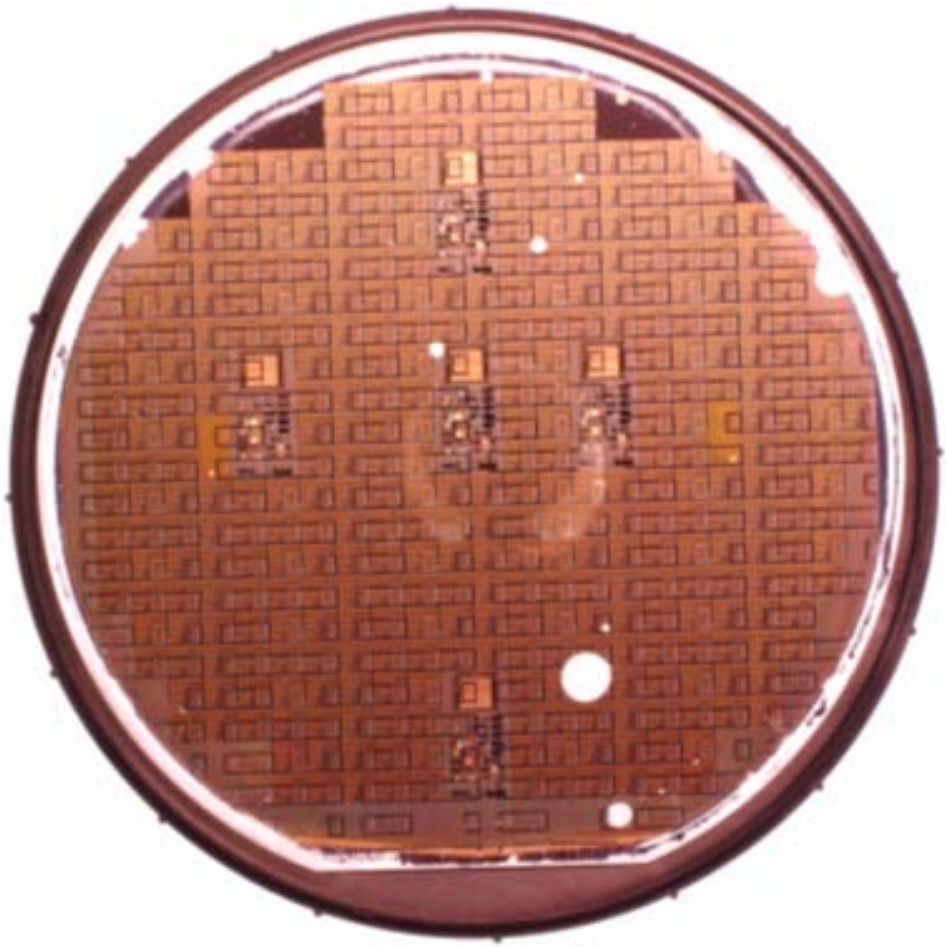
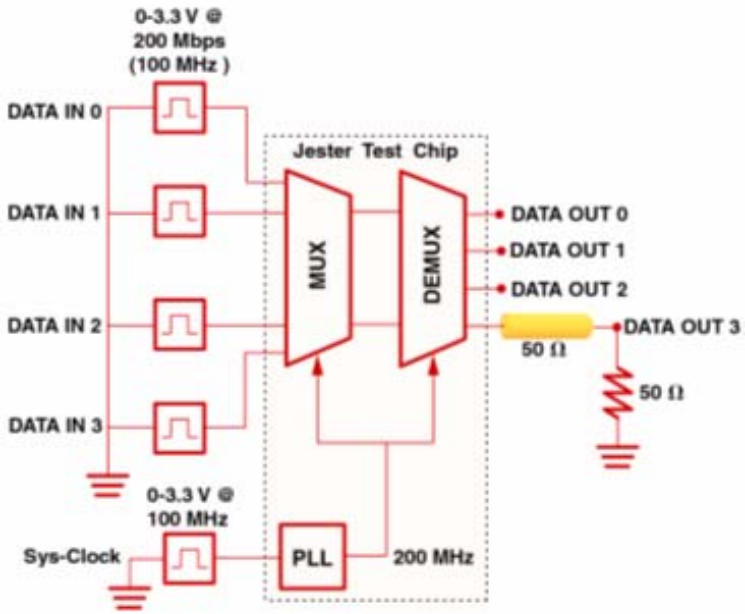
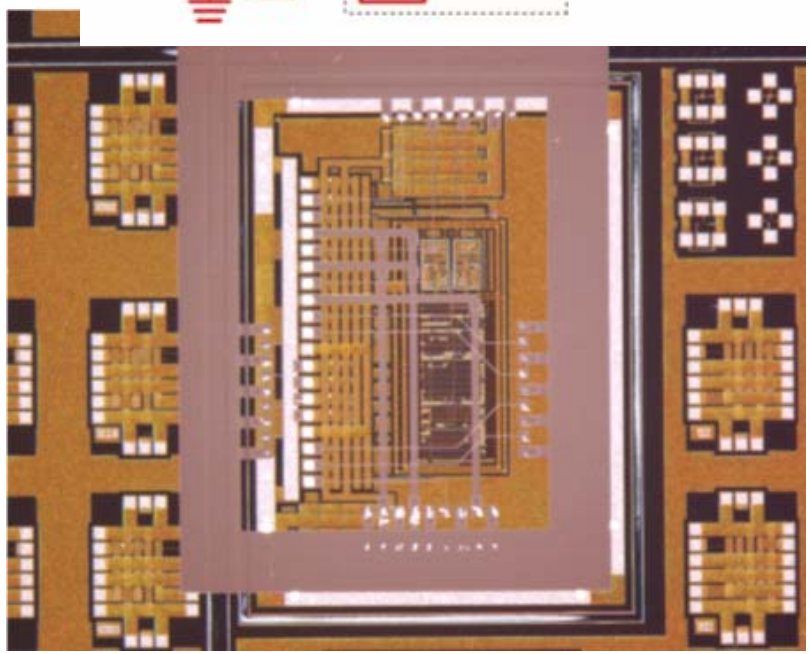
Bonded Active Circuits







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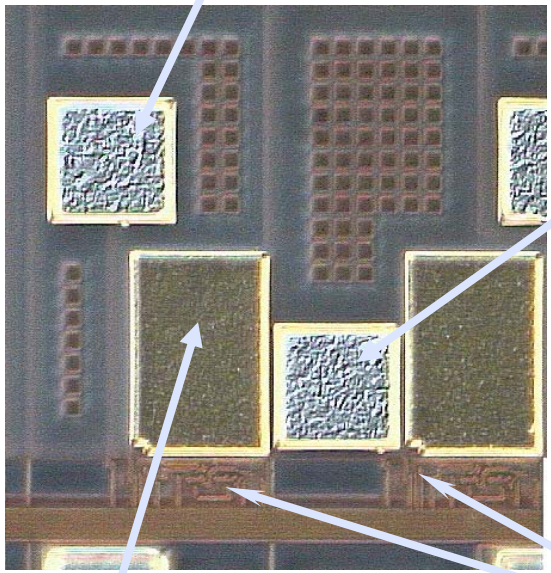
HGI Microsystems: Integrated IR/UV

GeorgiaTech/HRL/U Wisconsin

MWIR detector contact

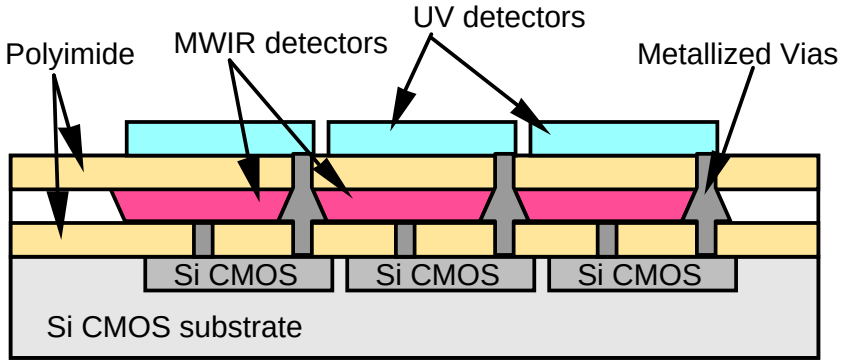


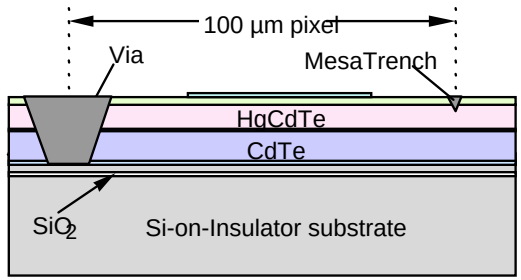
UV detector contact

Digital Si CMOS per-pixel ADC circuits

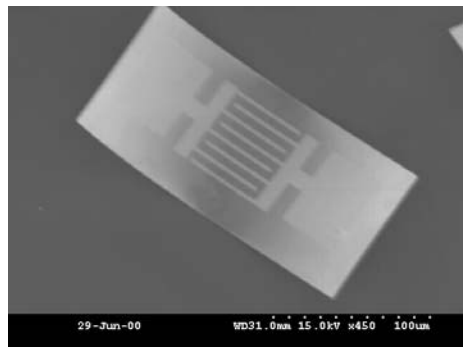
Capacitors

Single Pixel of Si circuit





MCT IR detector on SiO_2



GaN MSM UV detector on SiO_2

First Demo of thin GaN and MCT on Silicon, ADC and integrator functional, low T bonding, GaN MSM on Si worked as well as bulk version

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Layer Bonding

+ Bond layers of almost anything to anything
+ Low temperature, low stress process
+ Solution for heterogeneous circuits

- Layer alignment precision of about ¼ um with current tools (1 um is typical)
- Interconnection process
- Difficult handling of thinned layers and placing thinned bare chips on large diameter silicon wafers

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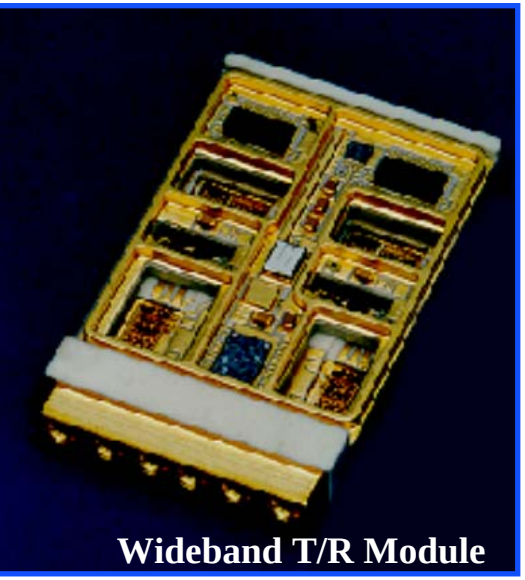
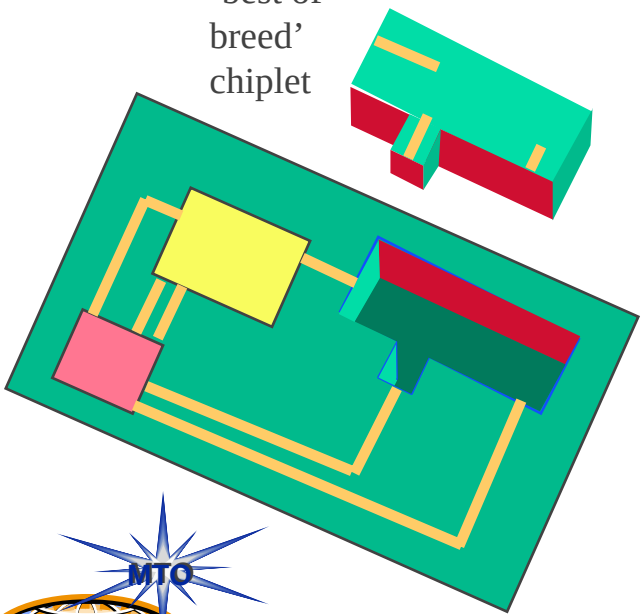
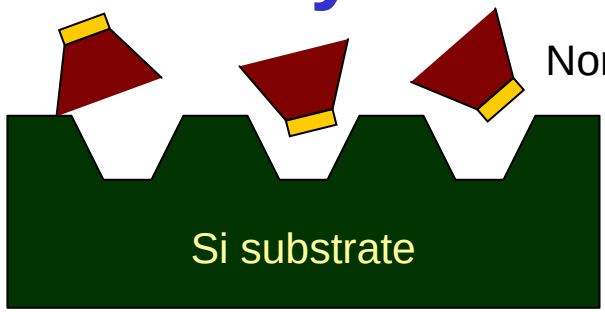
HGI: Fluidic Assembly



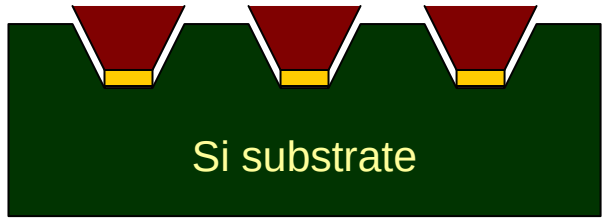
'best of breed' chiplet



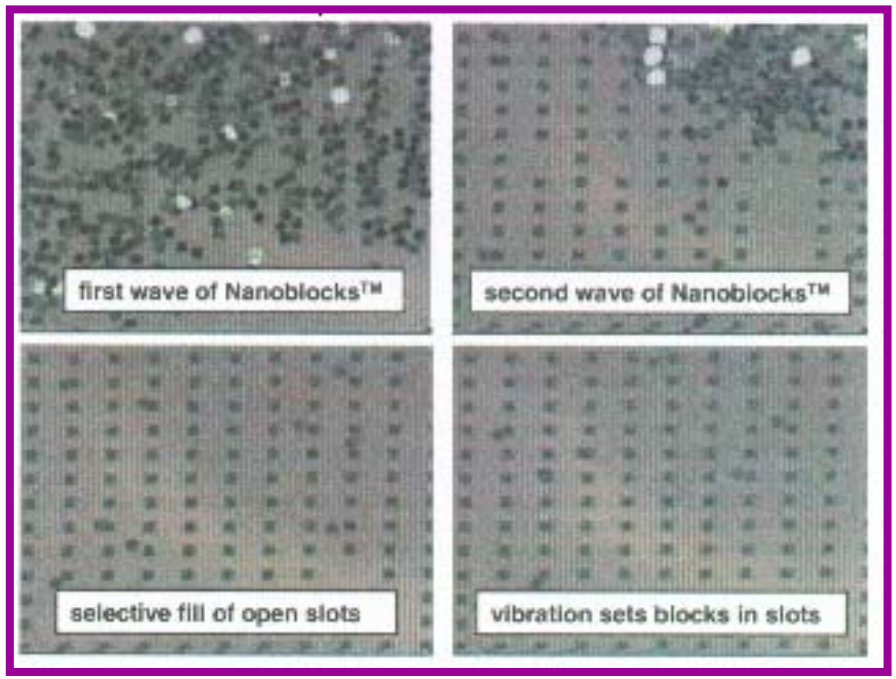
Northrop/Alien Technologies/UCSB



1. Fluidic assembly



2. Integrated devices



FSA for Parallel Assembly, Good Yield Experimentally With Sawed Chiplets

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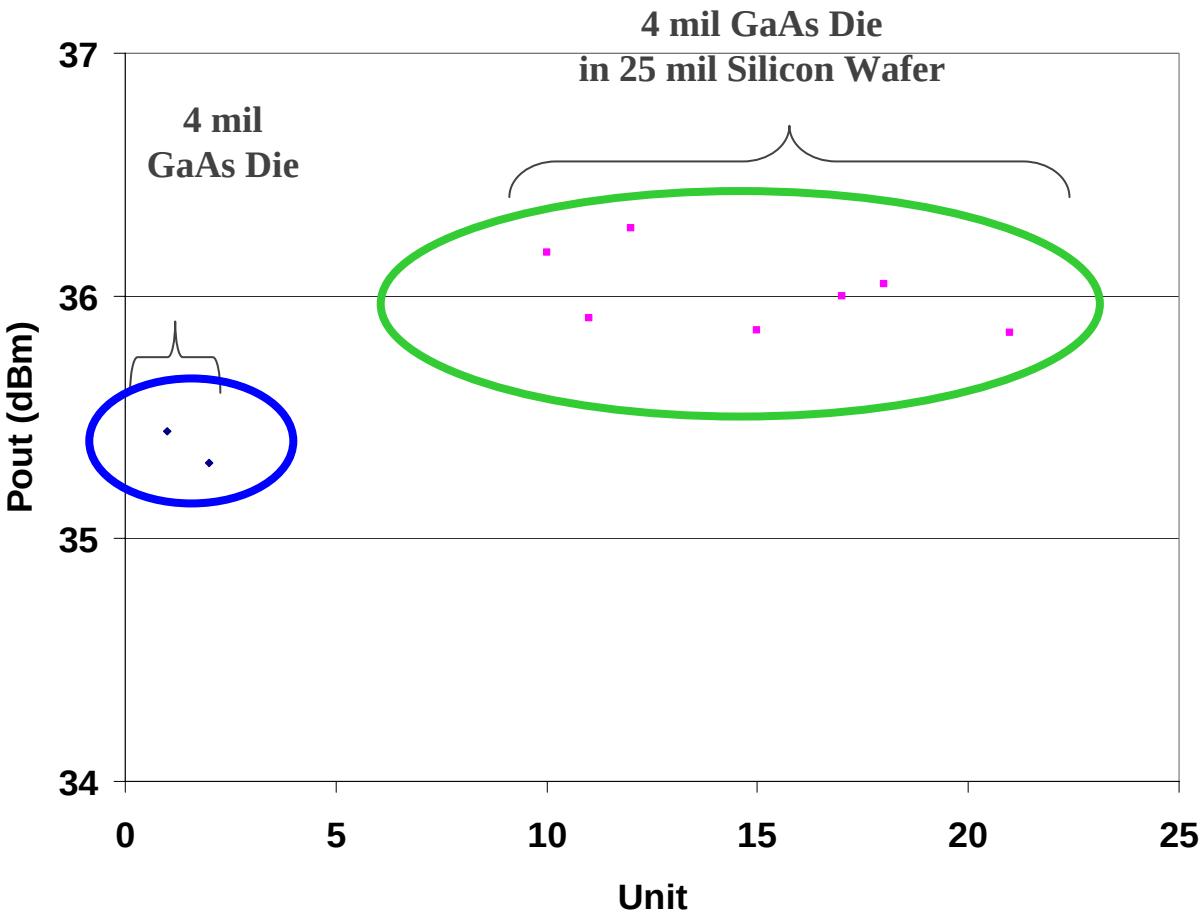
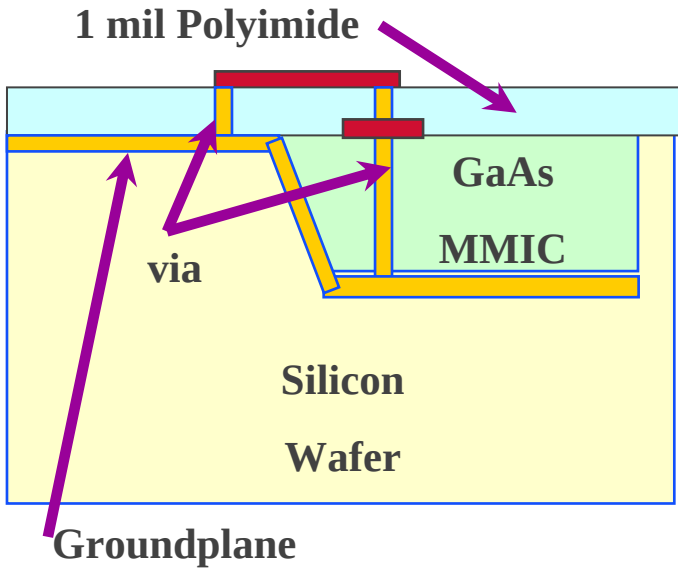
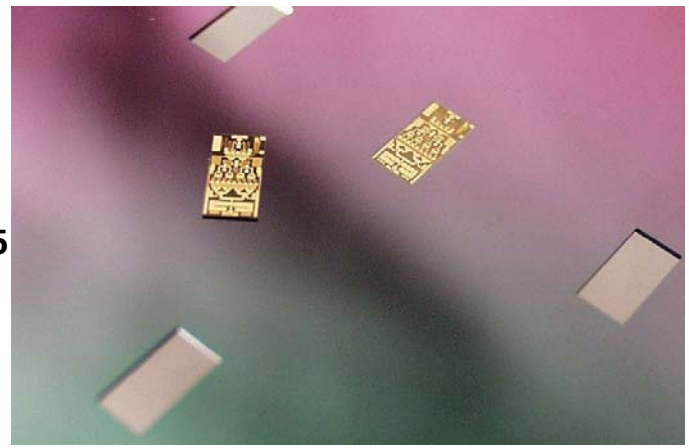
GaAs Power MMICs Demonstrated Similar Power Levels in a Silicon Wafer







GaAs chip in Silicon Wafer

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Fluidic Assembly

+ Can handle chips from any type of semiconductor
+ Parallel assembly process, can be enhanced

- High yield of assembly requires either lots of chiplets or recirculation where mechanical damage occurs

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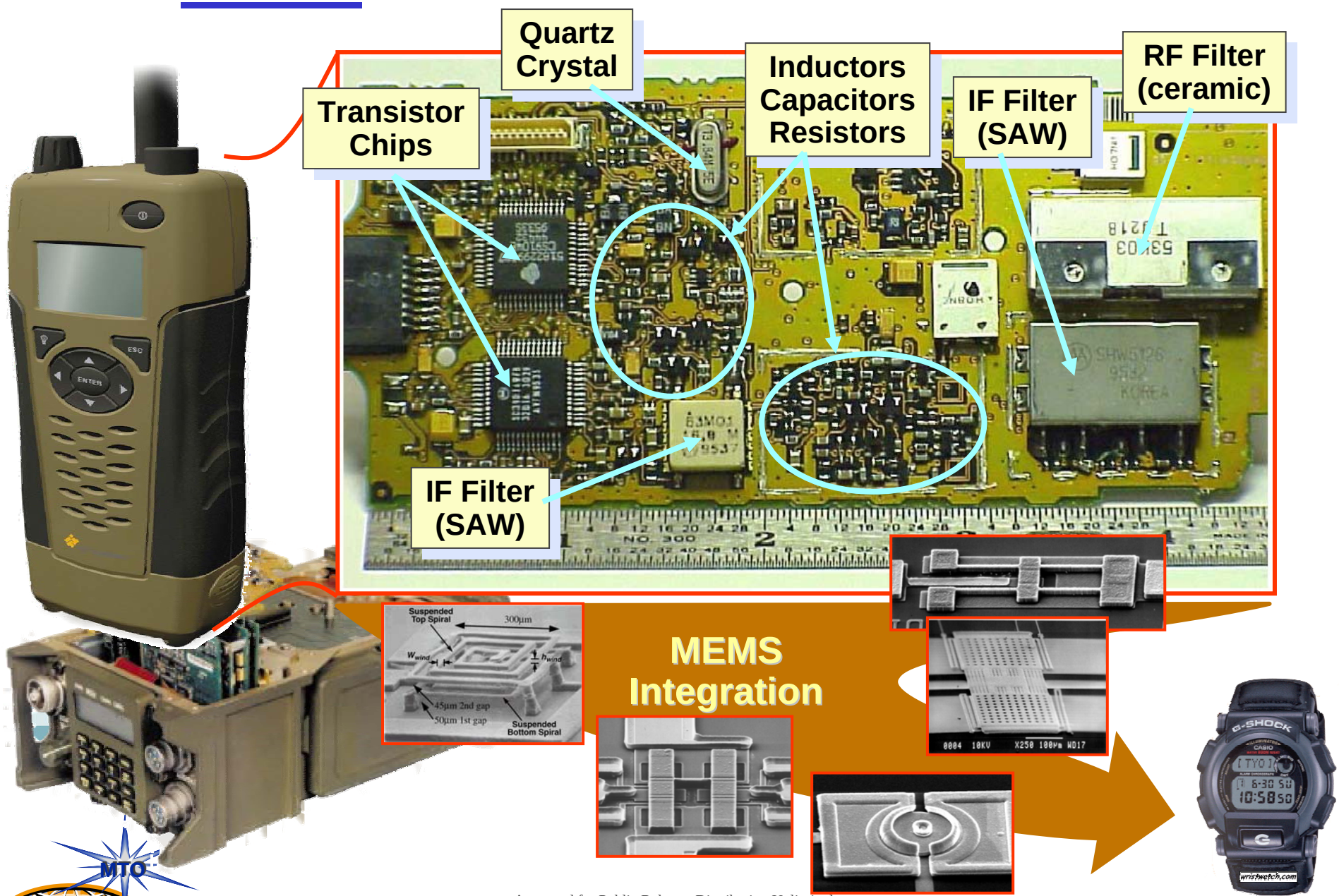
MEMS Provides Size Reduction



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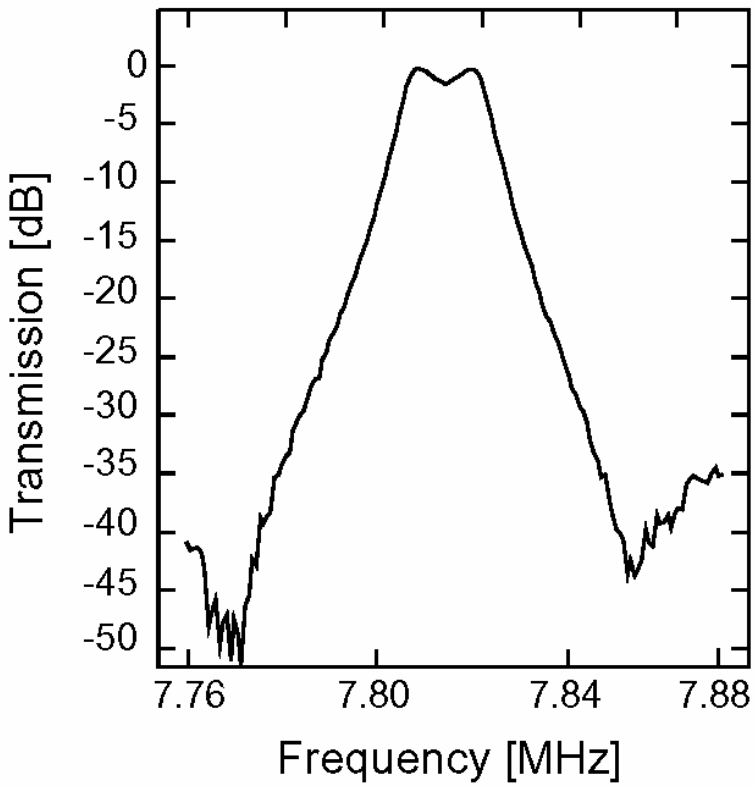
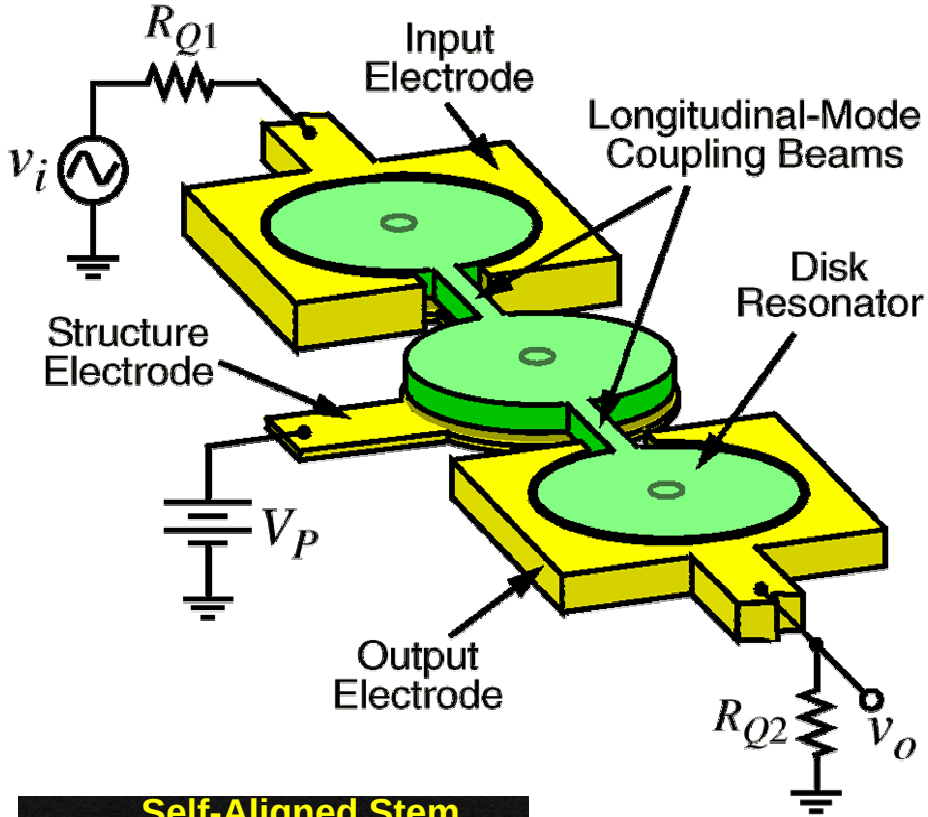
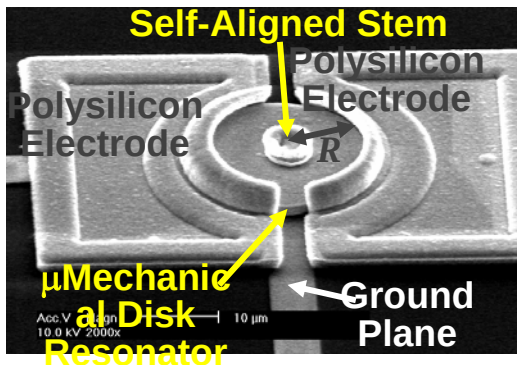
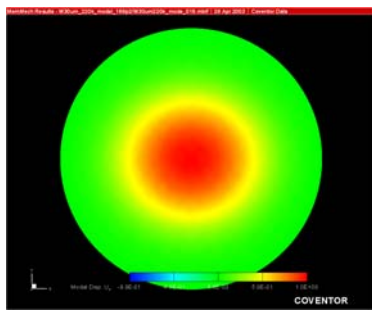
NMASP: μMechanical Filters

- Lower the impedance of GHz micromechanical resonators
- Create μmechanical circuits using such resonators

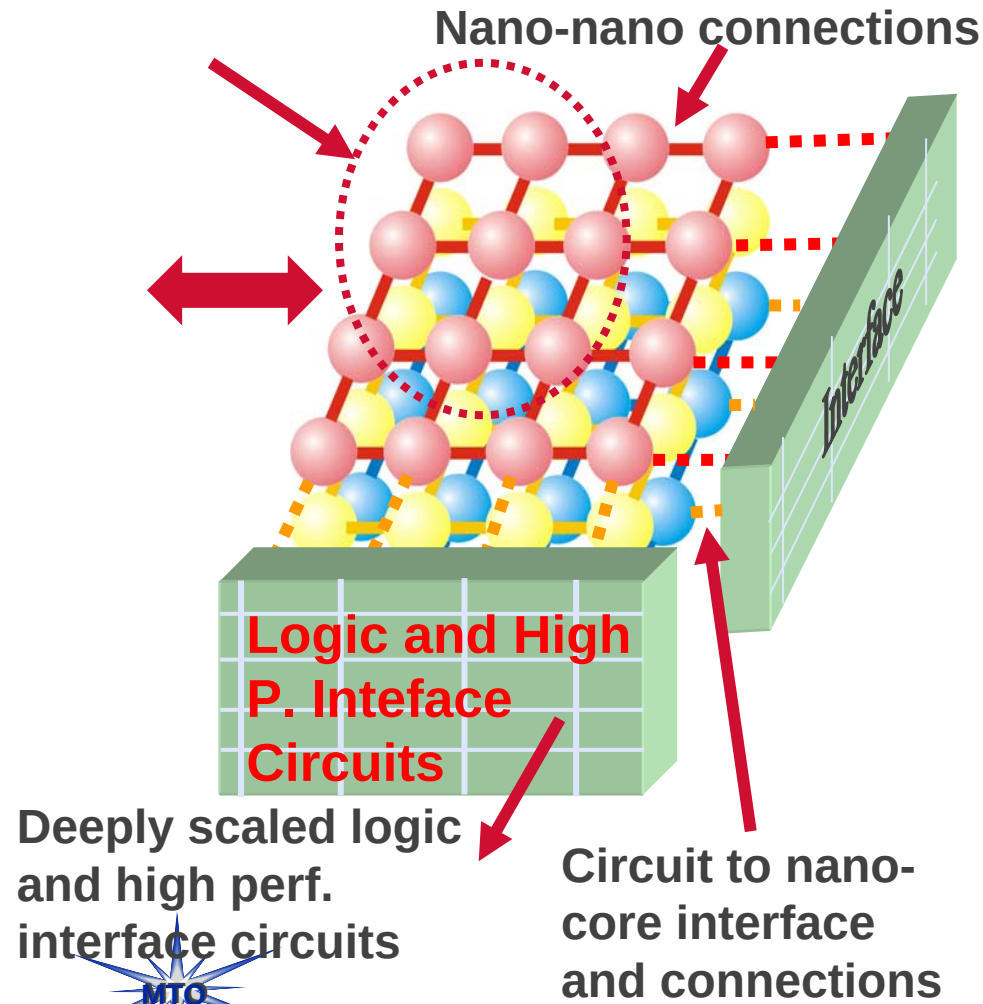








Future for 3D: A Platform for Nano



Challenges:

- Space transformation
- Interface/signal conversion and noise
- Assembly vs. lithographic fabrication

Potential approaches:

- Multi-walled Carbon nanotubes
- Sub-wavelength optical/plasmon
- Electromagnetic
- Modulated electron beam

Killer App here is massive memory with processing

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