Nitride Electronic NeXt-Generation Technology (NEXT)

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Industry Day

3 December 2008

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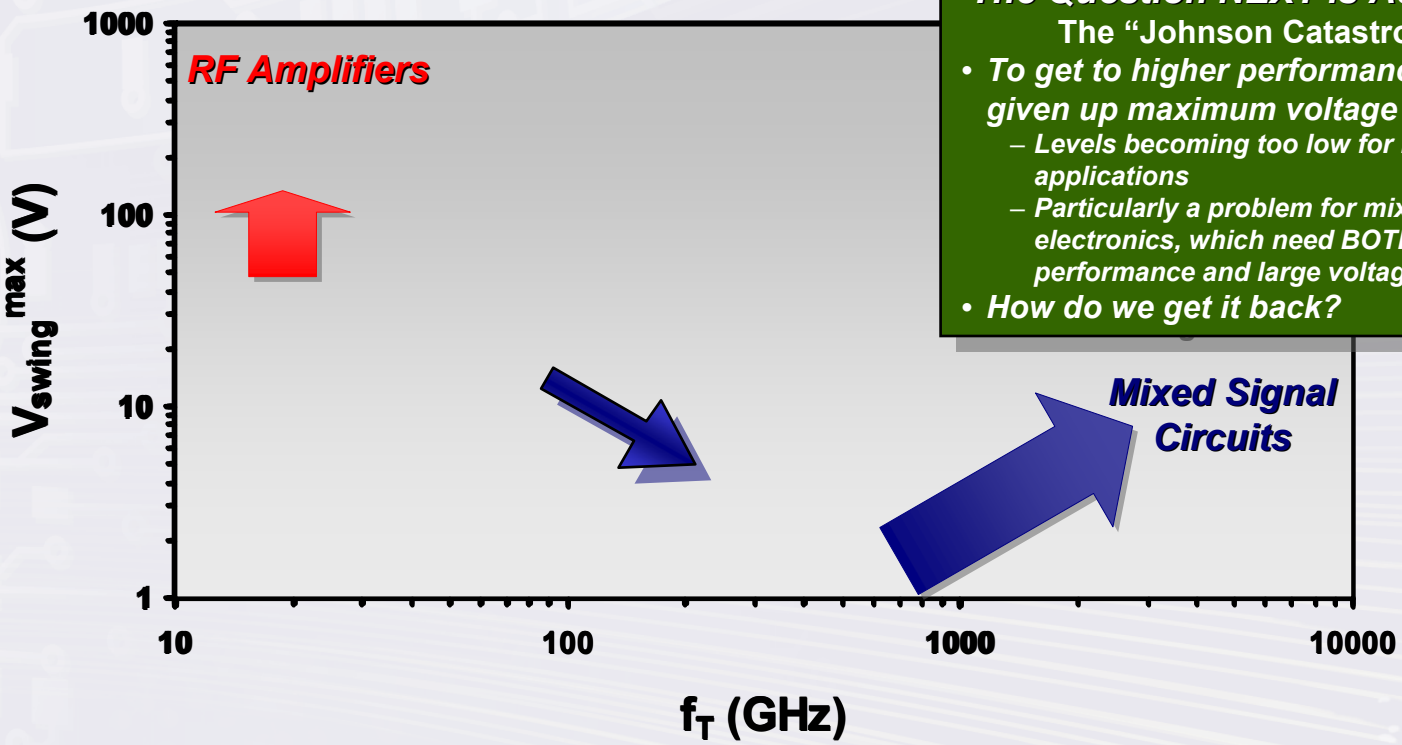
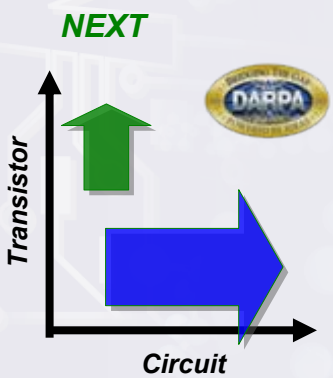
The Future of High Performance Analog and Mixed-Signal



The Question NEXT is Addressing

The "Johnson Catastrophe"

- *To get to higher performance, we have given up maximum voltage swing*
  - *Levels becoming too low for many applications*
  - *Particularly a problem for mixed-signal electronics, which need BOTH high performance and large voltage swing*
- *How do we get it back?*



Potential Approaches

- *Revolutionize the transistor*
  - *Develop a transistor technology able to achieve high f_T with high voltage swing*
- *Design around the problem*
  - *Develop a circuit approach which is much more tolerant of the inherent max voltage swing limits of the transistor*

NEXT

What it Requires

- *Ultra-small dimensions*
  - *"Si-like" device structure*
- *Logic capability*
  - *Enhancement mode*
- *LSI integration level*
  - *High transistor yield*
  - *Uniformity*

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Why GaN?

Parameter	Why?	Unit	Si	GaAs	ABCS [1]	InP [2]	GaN [3]
V_{peak}	Transit time	10^7 cm/s	1	2	8	2.5	2.5
E_{BK}	Voltage swing	10^5 V/cm	5.7	6.4	0.4	4	40
E_g	Charge density	eV	1.12	1.42	0.35	0.74	3.4
κ	Heat removal	W/cm·K	1.3	0.5	0.27	0.05	2.9

1. InAs channel
2. InGaAs channel
3. SiC substrate

The most important materials parameters for mixed-signal transistors favor GaN

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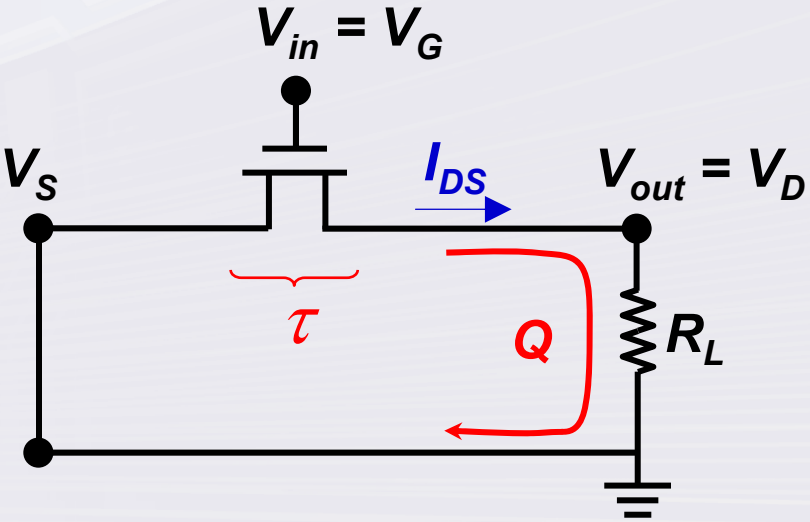
The Transistor: A Voltage Gain Device



$$\text{Gain} = V_{out} / V_{in}$$

$$= I_{DS} \cdot (R_L / V_G) = g_m / g_d$$

$$= \boxed{(Q/\tau)} \cdot \boxed{(R_L / V_G)}$$

An equivalent way of expressing the problem

Set by the application

The FOM of a transistor

Q = Total charge sent through the load

τ = Time required for charge to travel through the transistor

g_m = Transconductance = $\partial I_{DS}/\partial V_G$

g_d = $\partial I_{DS}/\partial V_D$

Transistor (1947)

"This is an abbreviated combination of the words 'transconductance' or 'transfer', and 'varistor'. The device logically belongs in the varistor family, and has the transconductance or transfer impedance of a device having gain, so that this combination is descriptive."

– Bell Telephone Laboratories Technical Memorandum (May 28, 1948)

Since 1947, the key challenges for transistors: Increase Q, decrease τ

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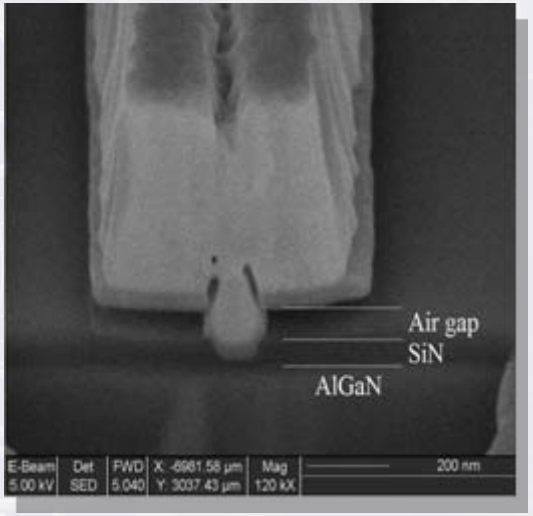
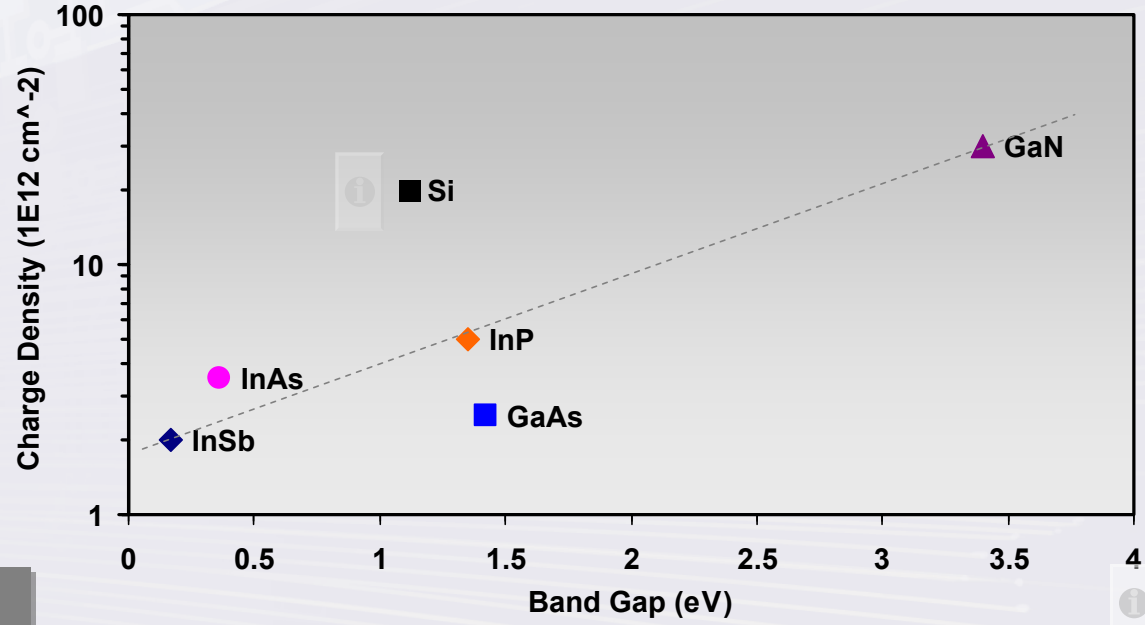
Maximizing Q





High Electron Mobility Transistor (1980)

Jpn J. Appl. Phys. 19, p. L225 (1980)

Maximize Q by locating a high density 2DEG close to the channel

Set by the material

$$I_{DS} = \frac{Q}{\tau} = \frac{e \cdot n_{2DEG} \times W_G \times L_{CH}}{\tau}$$

GaN is attractive because it offers extremely high charge density

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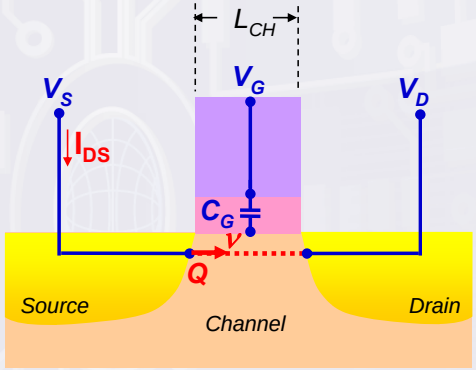
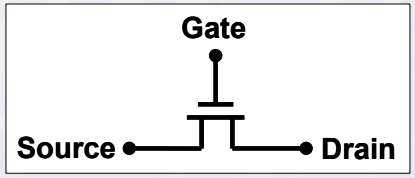
Minimizing τ

Idealized Transistor





$$\tau = \frac{L_{CH}}{v}$$

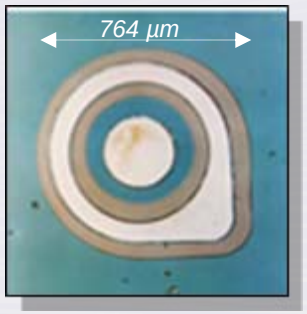
- L_{CH} ← *Minimize, through dimension scaling*
- v ← *Maximize, through materials choice*

L_{CH} = Channel length (i.e., the effective gate length)
v = average velocity of carriers across channel

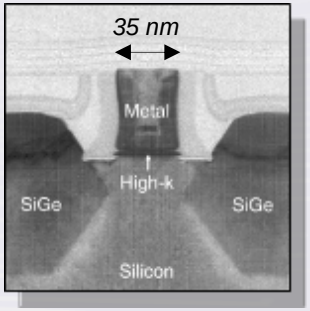
Dimension Scaling

How τ has been minimized since 1950s

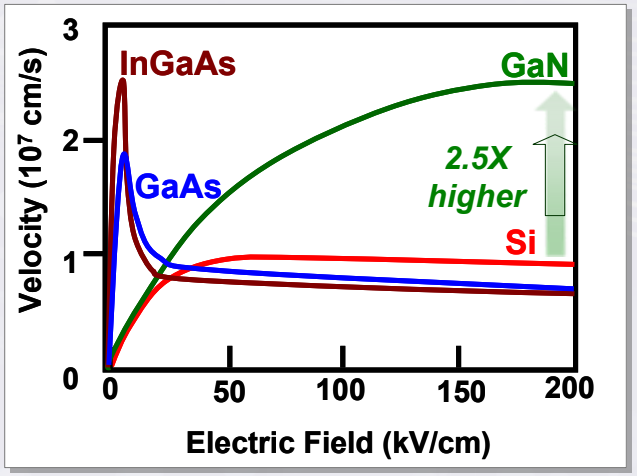
1950s
First commercial silicon planar transistor



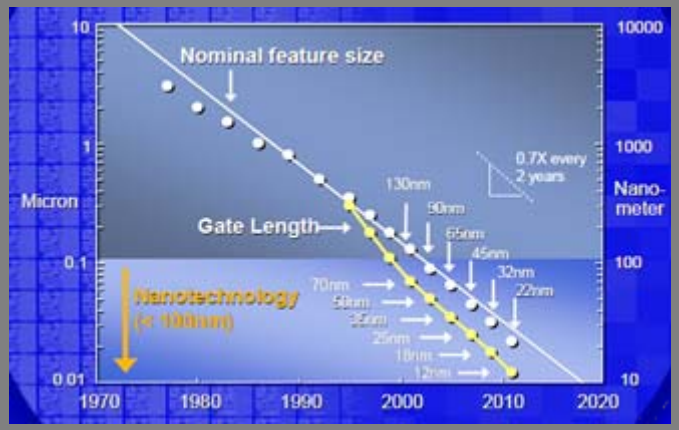
2007
Intel's 45nm-node MOSFET



Electron Velocity in Semiconductors



Moore's Law



GaN also offers the potential to decrease τ (for a given channel length)

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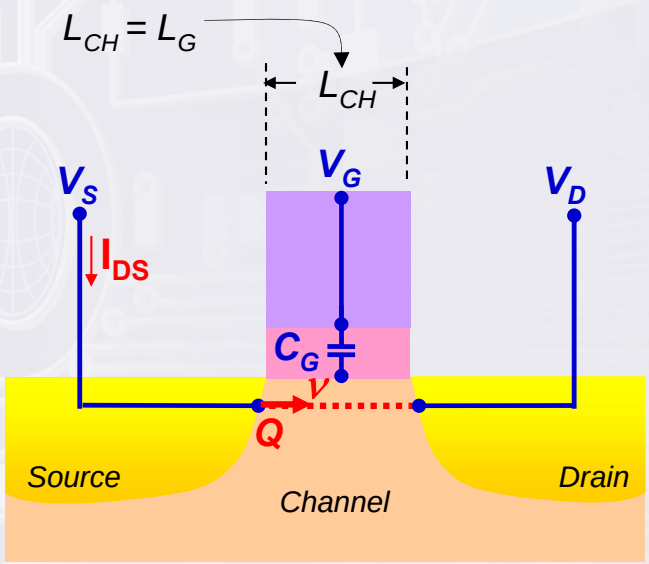
What Really Limits τ ?

Idealized Transistor



$$\tau_{total} = \tau_{L_G} = \frac{L_G}{v}$$

Challenge	Limitation	Today	NEXT
Reduce L_G	Lithography	L_G ~ 150 nm	L_G < 30 nm

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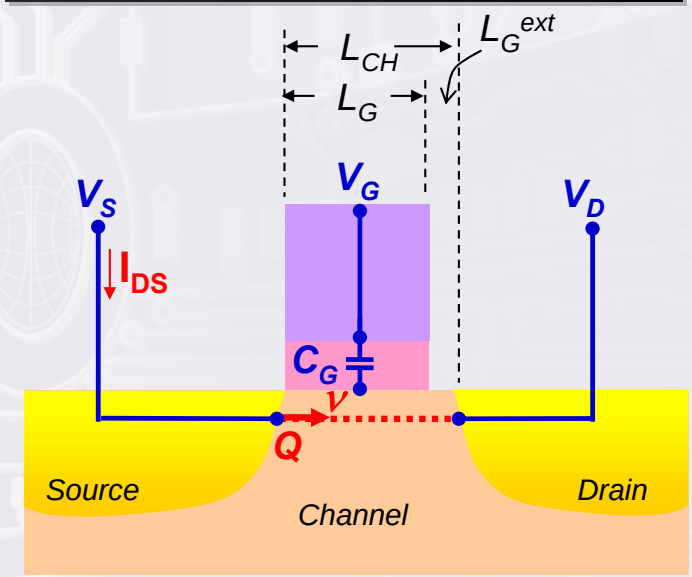
What Really Limits τ ?

More Realistic Transistor



$$\tau_{total} = \tau_{L_G} + \tau_{L_G^{ext}}$$

$$= \frac{L_G}{v} + \frac{L_G^{ext}}{v}$$

Challenge	Limitation	Today	NEXT
Reduce L_G	Lithography	L_G ~ 150 nm	L_G < 30 nm
Eliminate L_G^{ext}	$L_{CH} = L_G + L_G^{ext}$	L_G^{ext} > 40nm	L_G^{ext} < 3 nm

Challenge #1

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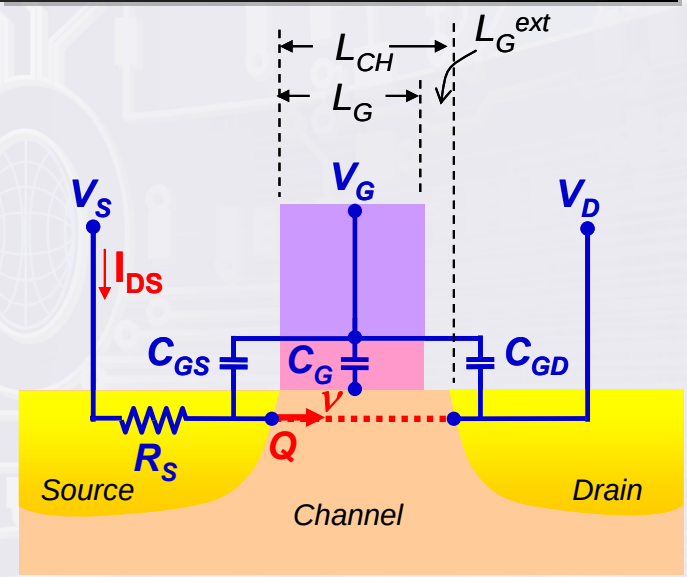
What Really Limits τ ?

Even More Realistic Transistor



$$\tau_{total} = \tau_{L_G} + \tau_{L_G^{ext}} + \tau_{R_S}$$

$$= \frac{L_G}{v} + \frac{L_G^{ext}}{v} + R_S(C_{GS} + C_{GD})$$

Challenge	Limitation	Today	NEXT
Reduce L_G	Lithography	L_G ~ 150 nm	L_G < 30 nm
Eliminate L_G^{ext}	$L_{CH} = L_G + L_G^{ext}$	L_G^{ext} > 40nm	L_G^{ext} < 3 nm
Reduce R_S	τ_{Rs}	R_S > 0.6 Ω·mm	R_S < 0.1 Ω·mm

Challenge #1

Challenge #2

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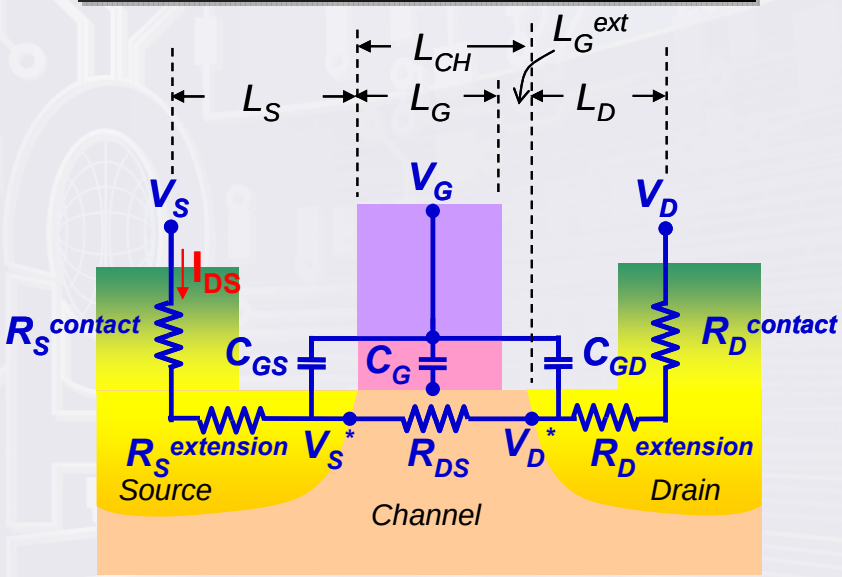
What Really Limits τ ?

Realistic Transistor



$$\tau_{total} = \tau_{L_G} + \tau_{L_G^{ext}} + \tau_{R_S} + \tau_{others}$$

$$= \left(\frac{L_G}{v} + \frac{L_G^{ext}}{v}\right)\left(1 + \frac{R_S + R_D}{R_{DS}}\right) + (R_S + R_D)C_{GD}$$

Challenge	Limitation	Today	NEXT
Reduce L_G	Lithography	L_G ~ 150 nm	L_G < 30 nm
Challenge #1 Eliminate L_G^{ext}	$L_{CH} = L_G + L_G^{ext}$	L_G^{ext} > 40nm	L_G^{ext} < 3 nm
Challenge #2 Reduce R_S	τ_{Rs}	R_S > 0.6 Ω·mm	R_S < 0.1 Ω·mm
Challenge #3 Reduce all other parasitics	τ_{others}	τ_{others} > 30 fs	τ_{others} < 10 fs

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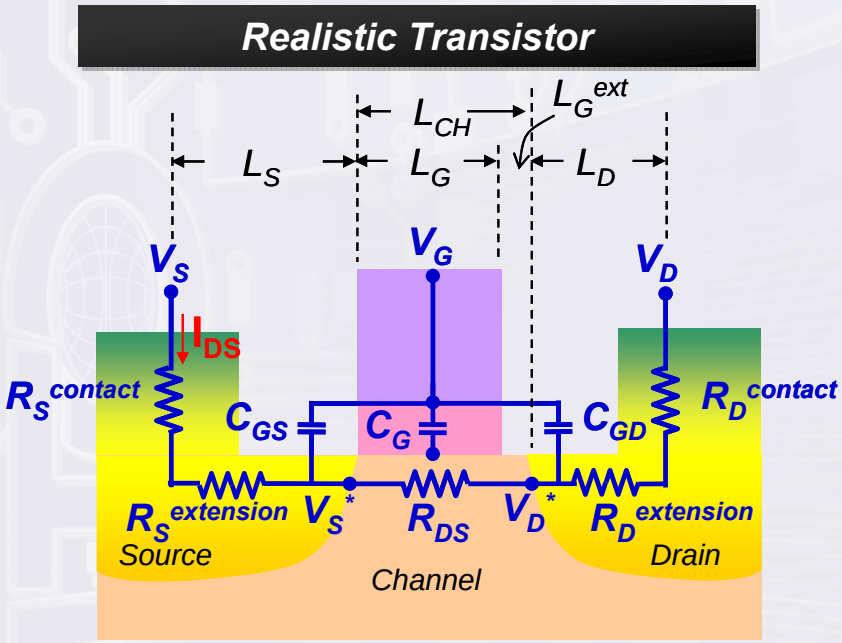
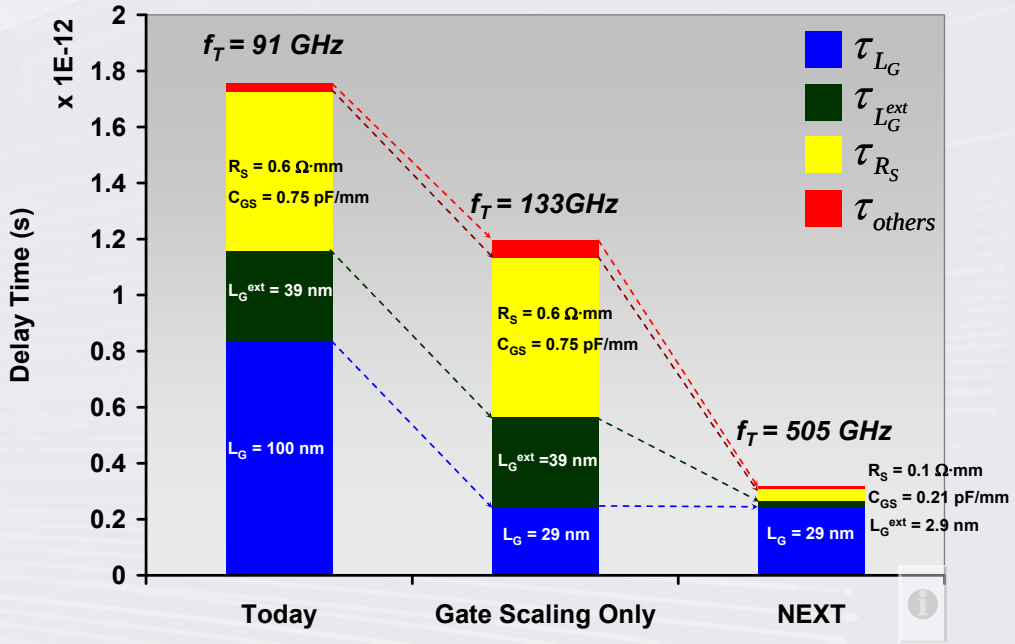
What Really Limits τ ?





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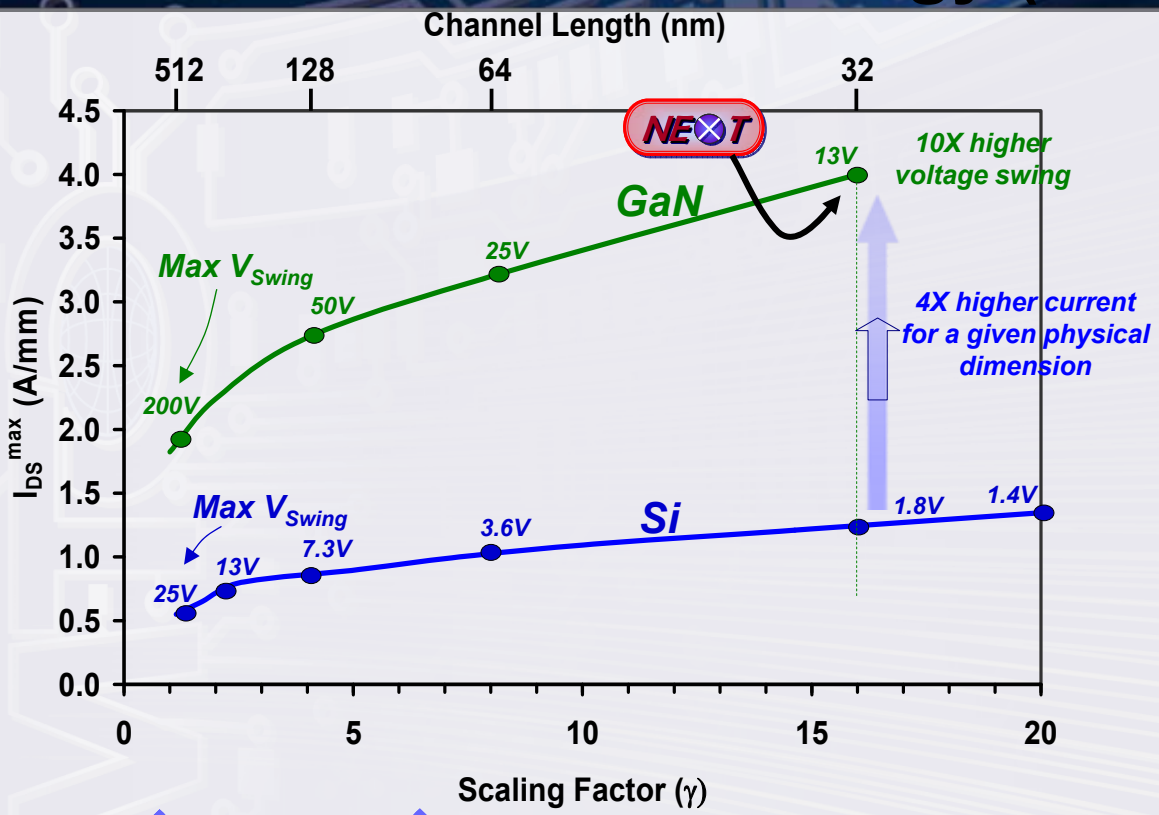

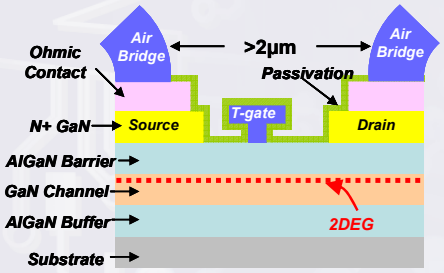

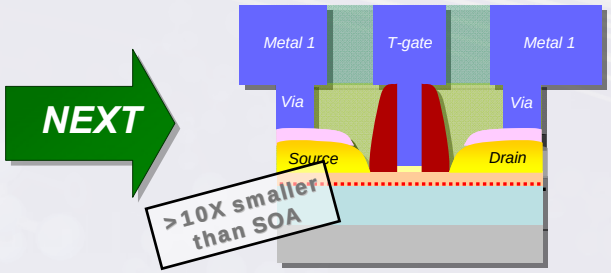

Program Objectives

- Develop a high performance nitride transistor for high speed RF, analog, and mixed signal electronics
  - I_{DS} levels 4X better than SOA Si
  - Voltage swings 10X more than Si
  - Enhancement mode operation
- Enable high integration level
  - High yield transistor process
  - Uniform
  - Reliable

Impact

- High dynamic range mixed-signal electronics
  - Would enable wideband power DACs with >100X increase in output power
  - Also enables 25 dB improvement in mixer IP3
- Enables complex E/D logic circuits
  - Ultra-low gate delay

NEXT will achieve 4 scaling generations in a single program to leapfrog Si

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Technical Challenges

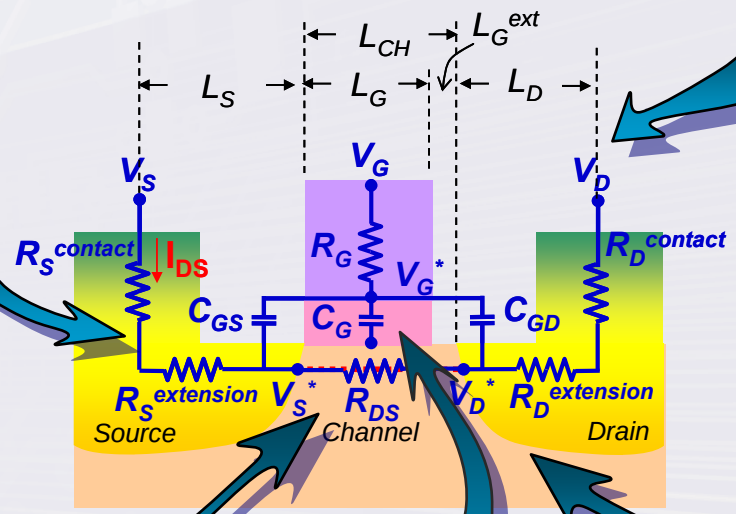
Challenge #2

Reduce Access Resistance

- Achieve low-resistance ohmic contact to source/drain
- Minimize / eliminate resistance of extension region

Uniformity/Yield

- Maintain uniformity and yield in highly scaled devices



Challenge #1

Minimize gate extension

- Minimize drain-side depletion region without sacrificing carrier velocity
- Maximize electric field along the channel while maintaining reliability

Enable E-mode Transistor

- Achieve and control high drain current in E-mode operation

Challenge #3

Control Other Parasitics

- Increase gate capacitor when scaling device
- Maintain or reduce all other parasitic capacitances

Problems facing nitrides resemble those in early days of Si MOSFET

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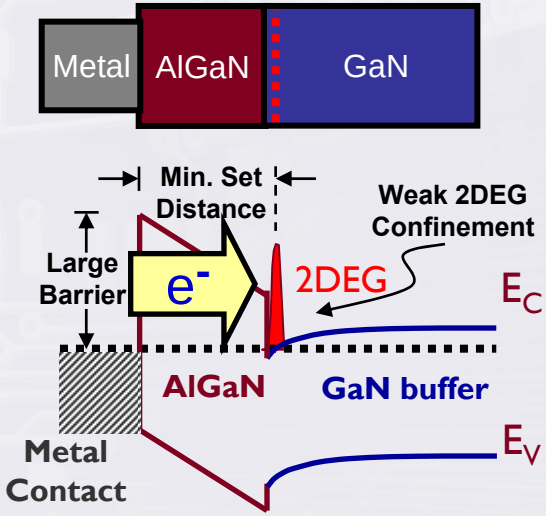
Limiting Physics in GaN HEMTs



Key Physics: 2DEG density determined by AlGaN thickness

Characteristics	Status
Gate length scaling	No
Access resistance	High
Charge confinement	Requires Back Barrier
E-mode operation	Limited

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Technical Approaches

Challenge #2

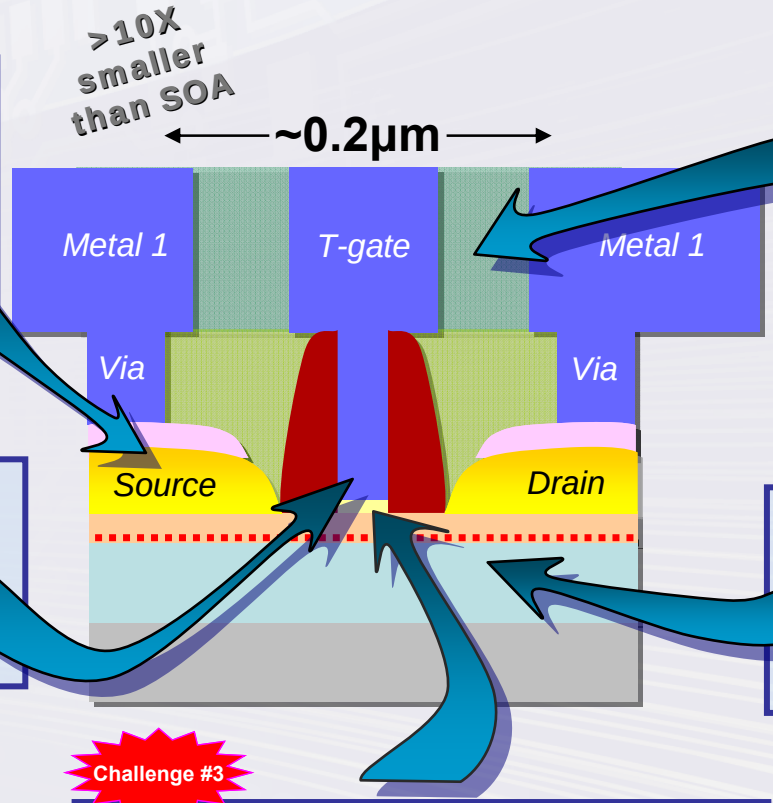
Reduce Access Resistance

- Epitaxial re-growth techniques at source & drain
- Optimize work function
- Ion implanted contacts

Challenge #1

Minimize gate extension

- Self-aligned device (like a Si MOSFET)
- Ultra short gate length (≤30nm)



Uniformity/Yield

- Self-aligned device
- Improved manufacturing methods

Enable E-mode Transistor

- N-face GaN for superior 2DEG density
- Multilayer GaN heterojunctions

Challenge #3

Control Device Capacitors

- High-K gate dielectric in combination with a low parasitic electrode
- Minimize channel thickness
- Laterally asymmetric channel doping

Integration & performance will demand a silicon-like GaN transistor

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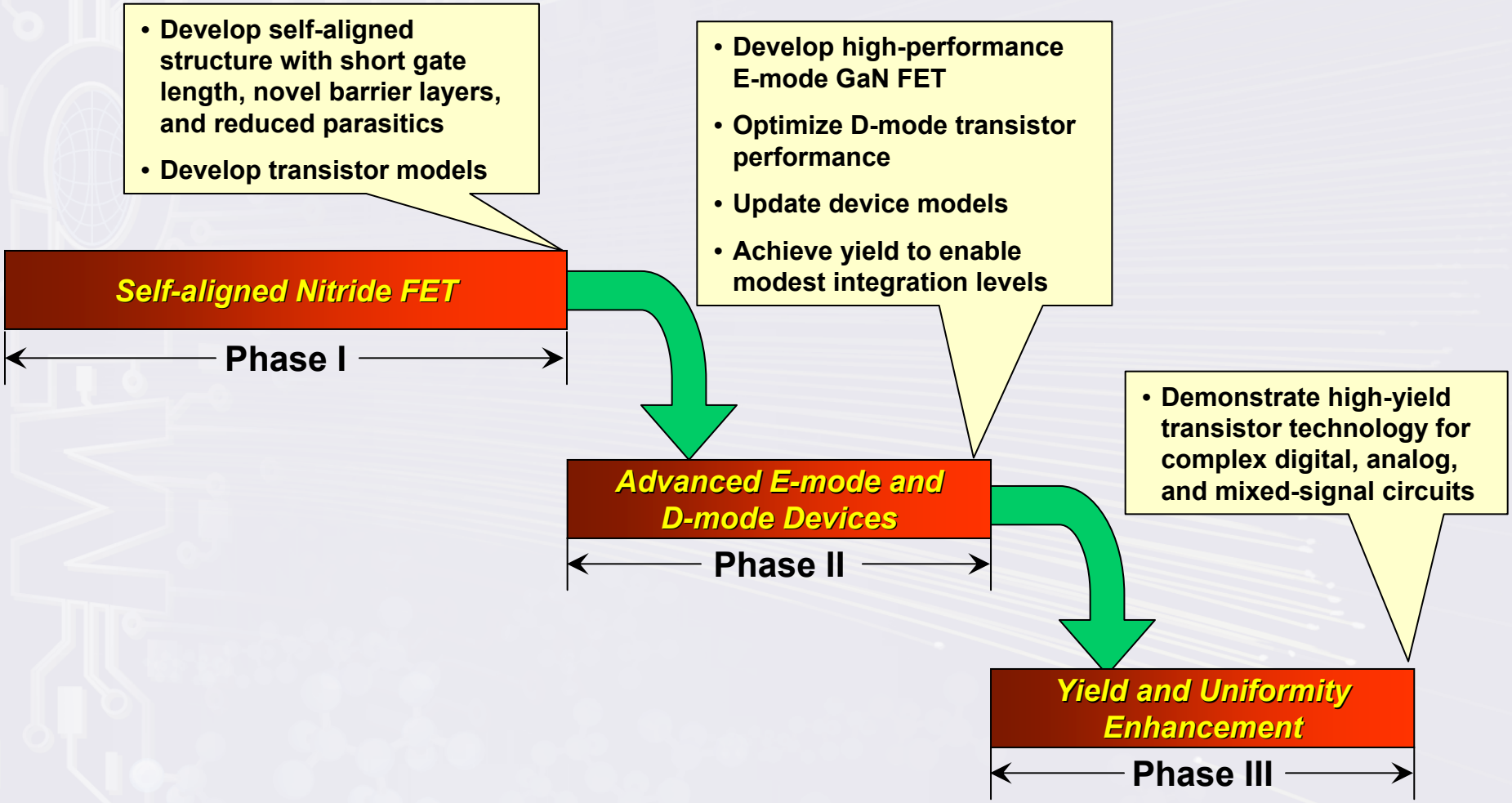
Program Schedule



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Program GNG Metrics

	Metric	Unit	Today	Phase I	Phase II	Phase III
Performance	D-mode f_T	GHz	150	300	400	500
	D-mode f_{max}	GHz	200	350	450	550
	D-mode Johnson FOM (1)	THz • V	N/A	5	5	5
	E-mode f_T	GHz	85	200	300	400
	E-mode f_{max}	GHz	150	250	350	450
	E-mode Johnson FOM (1)	THz • V	N/A	5	5	5
Yield	Transistor yield (2)	%	N/A	50 (3)	75 (3)	95 (4)
	PCM yield (5)	%	N/A	30 (6)	30 (7)	70 (8)
Uniformity	σ (V_{TH}) (9)	mV	N/A	50 (3)	40 (3)	30 (4)
	σ (f_T) (9)	GHz	N/A	50 (3)	40 (3)	30 (4)
	σ (f_{osc}) (9)	%	N/A	15 (6)	10 (7)	5 (8)
	Degradation Time (10)	Hrs	N/A	>10	>100	>1000

(1) Johnson FOM = (breakdown voltage) x (f_T)
(2) Yield defined as fraction of devices tested that meet f_T metric.
(3) Test sample: at least 100 devices on a single wafer.
(4) Test sample: at least 100 devices/wafer over a lot of at least 5 wafers.
(5) Yield defined as fraction of PCMs tested that achieve 80% of designed frequency.
(6) PCM to be a 5-stage ring oscillator. Test sample: at least 20 PCMs on a single wafer.
(7) PCM to be a 51-stage ring oscillator. Test sample: at least 20 PCMs on a single wafer.
(8) PCM to be a 501-stage ring oscillator. Test sample: at least 20 PCMs/wafer over a lot of at least 5 wafers.
(9) The standard deviation of the stated parameter.
(10) Minimum test time for PCM until failure condition observed. Test sample: 20 PCMs. Failure condition: Failure of a single PCM or average frequency changes by 20%.

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Some BAA Excepts

- *A proposal must address both Technical Areas of Interest in a comprehensive manner. Proposals that fail to do so will be considered not responsive.*
  - *Technical Area I: Highly-Scaled Nitride High Electron Mobility Transistor (HEMT) E/D Processes*
  - *Technical Area II: Large Scale Integration*
- *Proposers should describe, in detail, within their proposal how they plan to evaluate the demonstration circuits so that they can demonstrate that they have met all of the GNG requirements…*
  - *(6) PCM to be a 5-stage ring oscillator. Test sample: at least 20 PCMs on a single wafer.*
  - *(7) PCM to be a 51-stage ring oscillator. Test sample: at least 20 PCMs on a single wafer.*
  - *(8) PCM to be a 501-stage ring oscillator. Test sample: at least 20 PCMs/wafer over a lot of at least 5 wafers.*
- *Performers are expected to meet or exceed all GNG Metrics shown in Table 1 by the conclusion of each Phase. Proposers may, at their option, propose more ambitious values for any of the GNG Metrics than those indicated in Table 1. In general, proposals committing to the most aggressive GNG Metrics in each Phase will be preferred, provided that the risk in delivering the stated metrics, as described in the proposal, is considered reasonable by the reviewers.*
- *In addition to GNG Metrics, proposers are requested to propose additional metrics ("Proposer-Defined Metrics"). Such metrics may be specific to the particular approach and should provide insight into some of the secondary performance goals, particularly device goals, expected to be met by the end of each Phase consistent with achieving the program GNG Metrics.*

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More BAA Excepts

- ***Proposers must define a realistic schedule and budget*** ***that meets the metric and deliverable requirements. The proposed period of performance for each of these Phases and metric schedule will be included by Proposers within their technical proposals and will be factors considered as part of the source selection process (see below). In general, shorter Phases are preferable, but each Phase should clearly be adequate in duration to meet its objectives, assuming reasonable risks and at a reasonable cost. Proposals should discuss plans for managing these factors.***
- ***Program plans should include Proposer-Defined Metrics every six months.***
- ***Evaluation of proposals*** ***will be accomplished through a scientific/technical review of each proposal using the following criteria, in order of descending importance: (a) Ability to meet Program Go/No-Go Metrics; (b) Overall Scientific and Technical Merit; (c) Potential Contribution and Relevance to the DARPA Mission; (d) Realism of Proposed Schedule; (e) Proposer's Capabilities and/or Related Experience; (f) Plans and Capability to Accomplish Technology Transition; and (g) Cost Realism.***
- ***Proposal abstracts*** ***are encouraged in advance of full proposals in order to provide potential proposers with a rapid response to minimize unnecessary effort.***

Some Important Dates

• Proposal abstract due	17 Dec 2008
• Feedback from DARPA	16 Jan 2009*
• Full proposal due	17 Feb 2009

* Approx.

Discussion with the DARPA PM are allowed & encouraged

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