

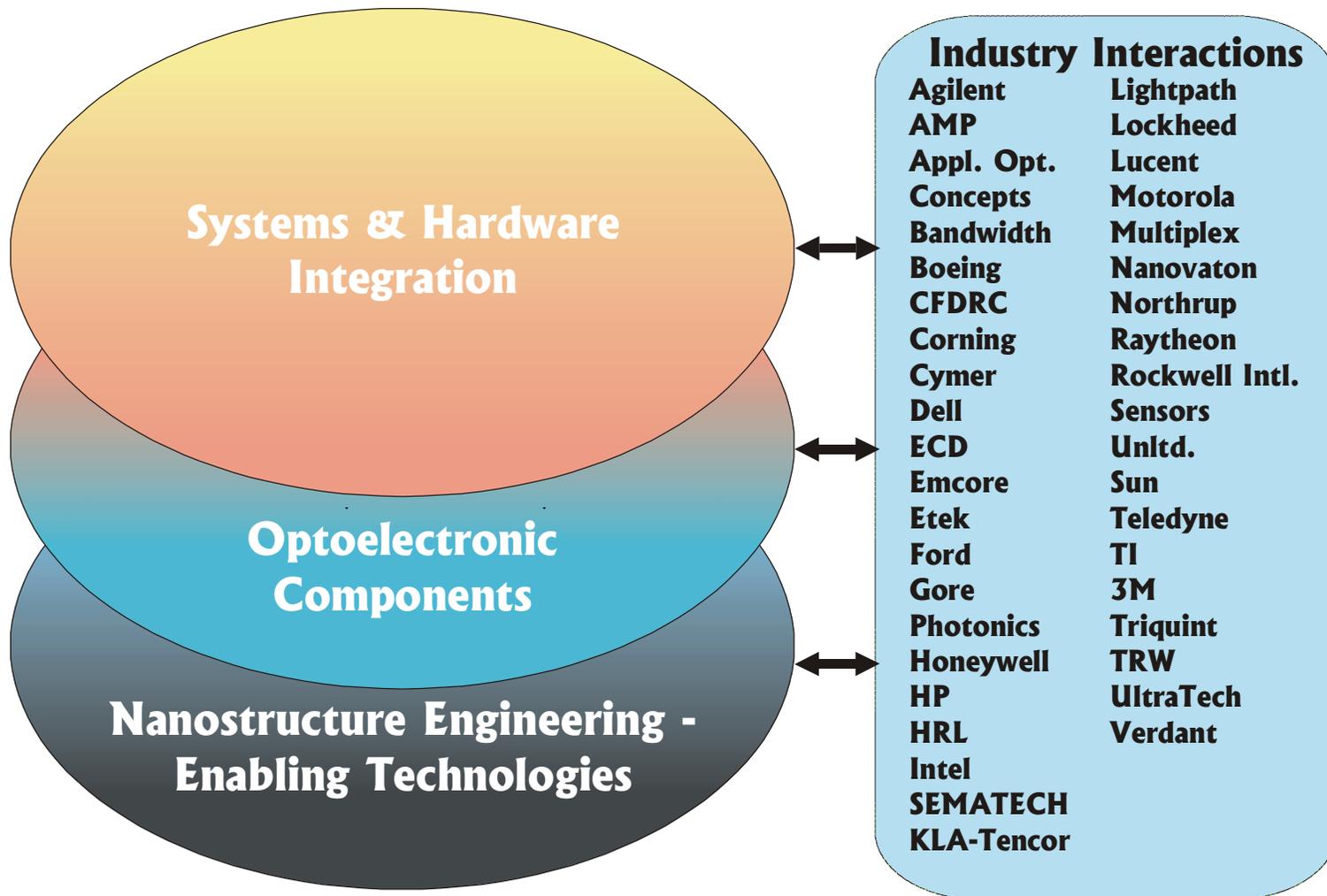


# HIGH CAPACITY OPTOELECTRONIC INTERCONNECTS

<p>STANFORD</p>  <p>STANFORD</p>	<p>UNM</p> 	<p>U. Illinois</p> 	<p>UT-Austin</p> 	<p>USC</p> 
<p>M. M. Fejer J. S. Harris M. Horowitz D. A. B. Miller</p>	<p>S. R. J. Brueck L. R. Dawson S. D. Hersee D. Huffaker R. K. Jain L. F. Lester K. J. Malloy M. Osinski</p>	<p>J. J. Coleman K. Choquette G. C. Papen</p>	<p>R. T. Chen D. G. Deppe</p>	<p>A. E. Willner</p>

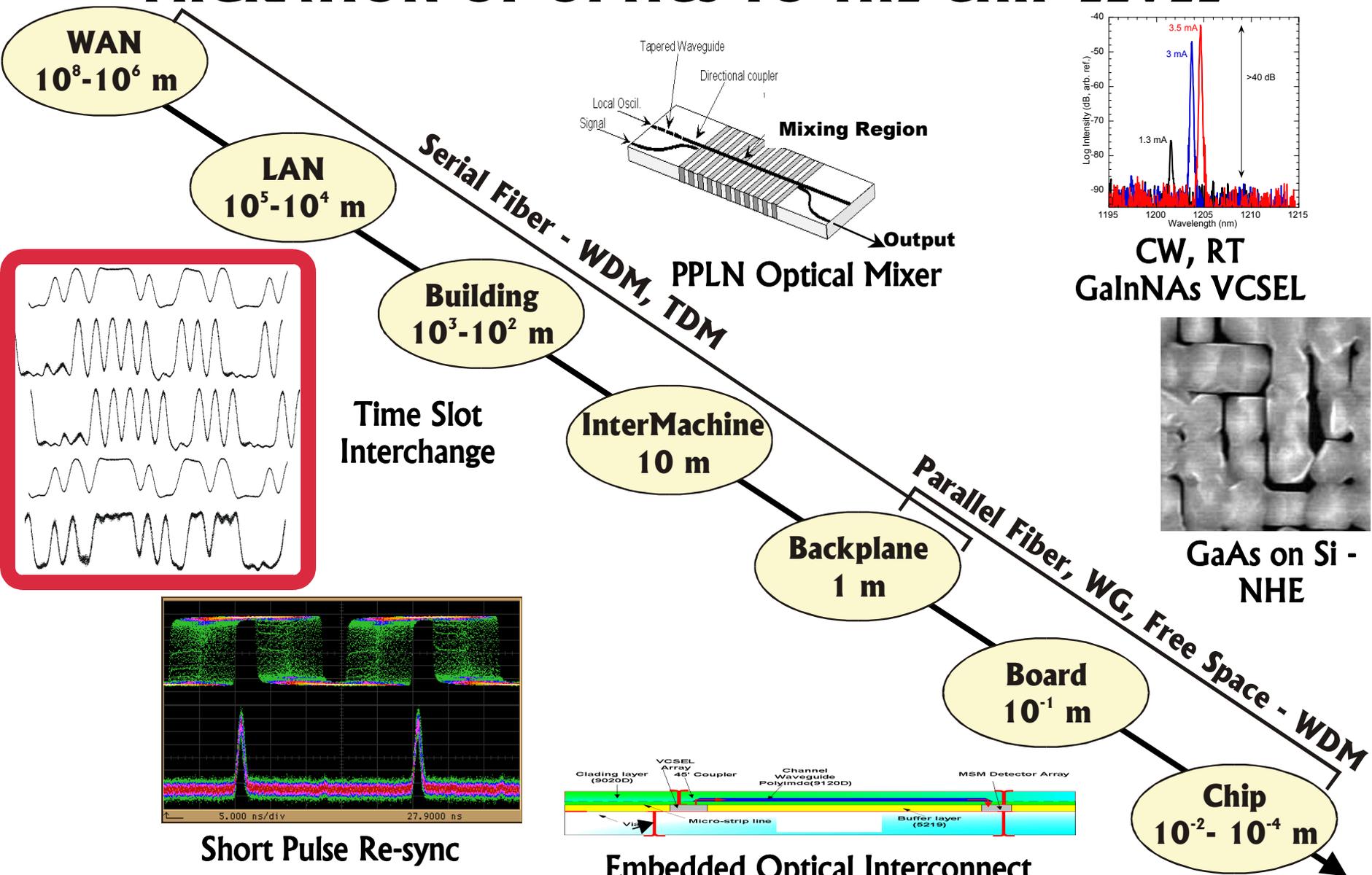


# **OMC RESEARCH EXTENDS FROM INTEGRATION TO DEVICES AND ENABLING TECHNOLOGIES**



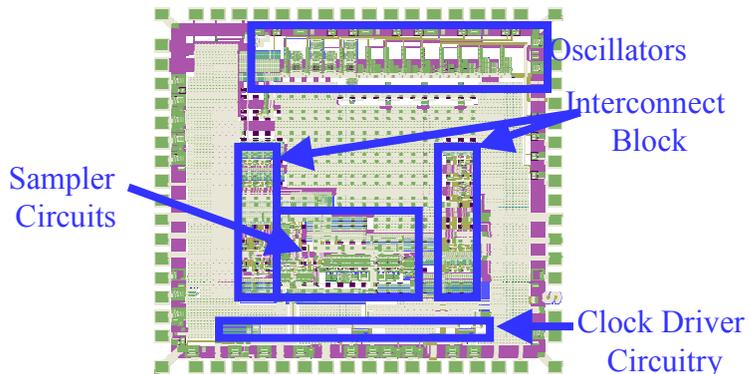


# MIGRATION OF OPTICS TO THE CHIP LEVEL

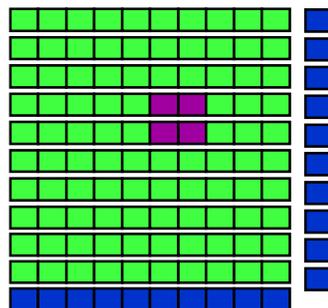




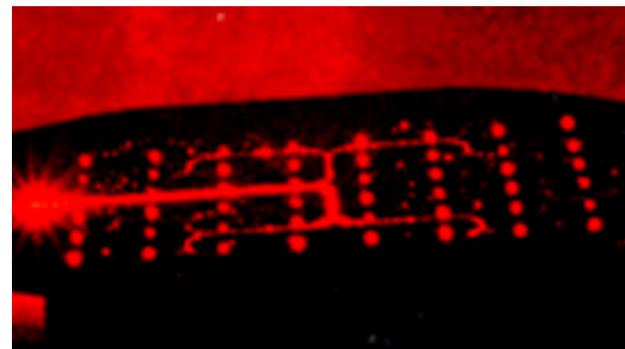
# SYSTEMS AND HARDWARE INTEGRATION



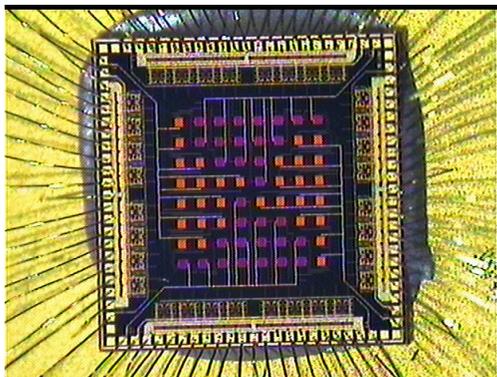
Latency Test Chip



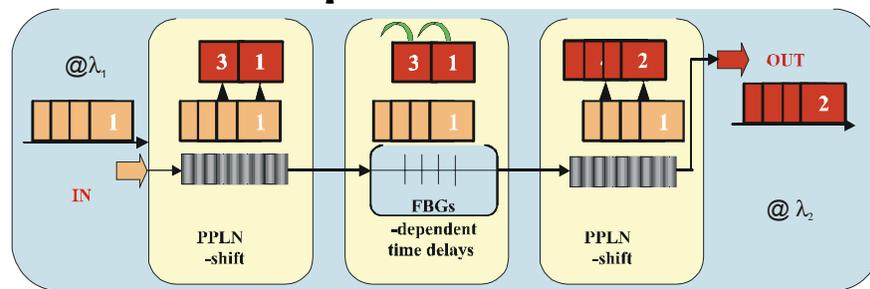
Error Correction  
and BER Studies



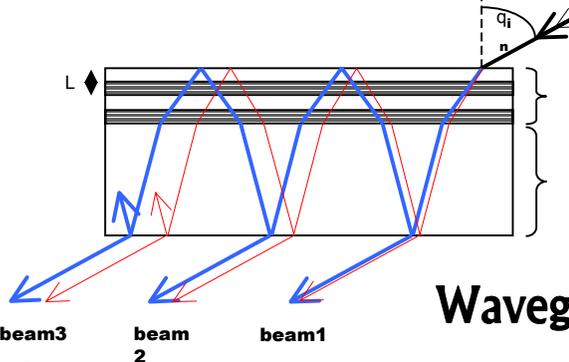
Optical Clock Distribution



8x8 VCSEL Array



Time Slot Interchange and  
Wavelength Conversion

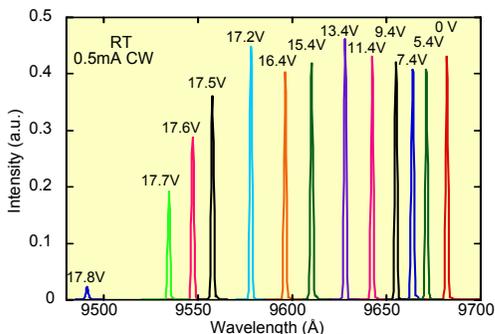


Waveguide WDM Components

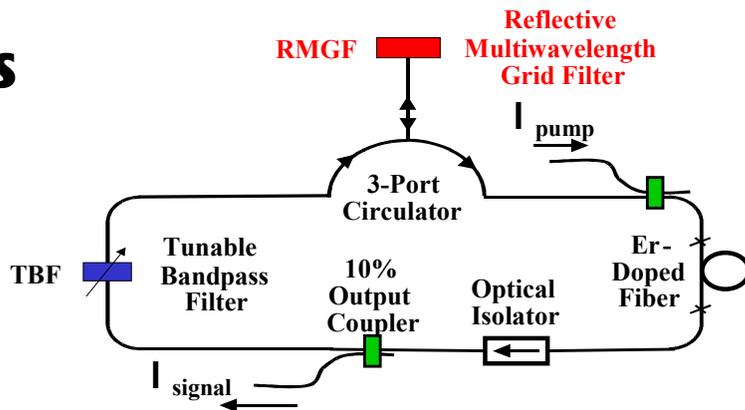


# OPTOELECTRONIC COMPONENTS

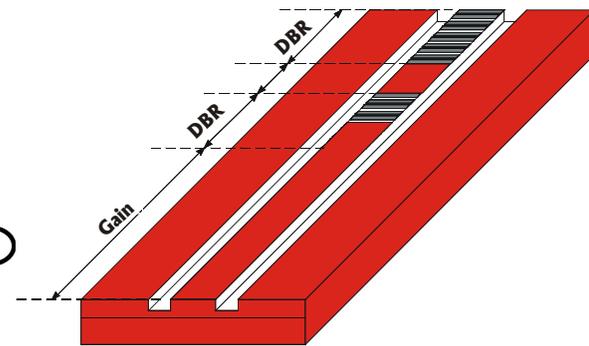
## Tunable Sources



MEMS-VCSEL

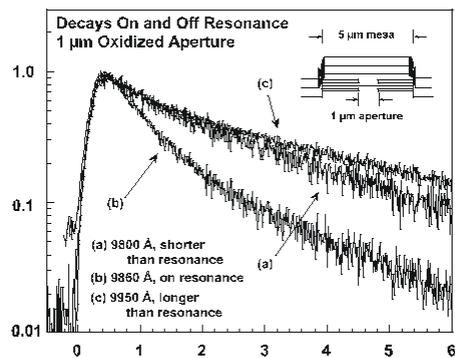


Fiber Laser

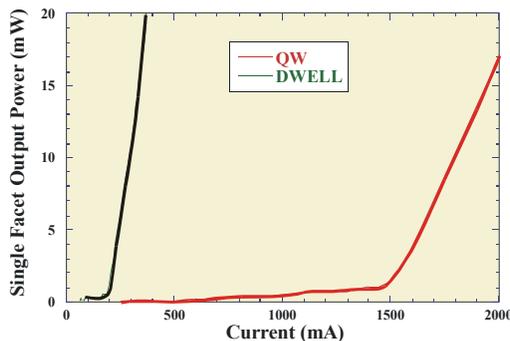


Two-Section OEIC

## Long-Wavelength Sources

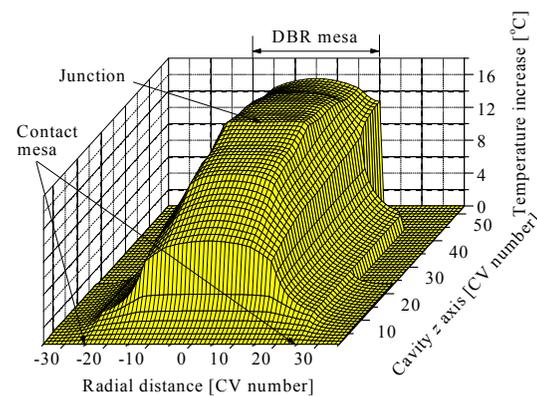


VCSEL Microcavity Effects



Quantum Dot Lasers

## 3D VCSEL Model

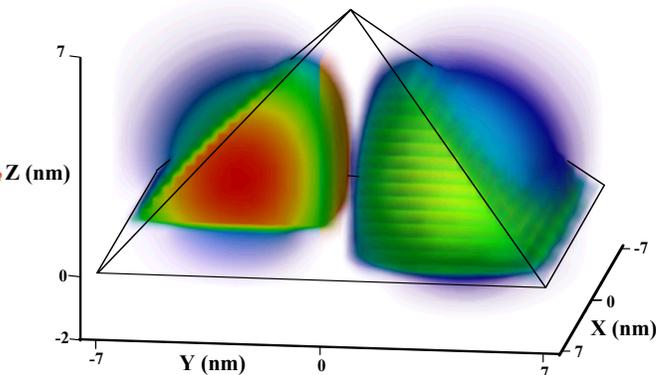




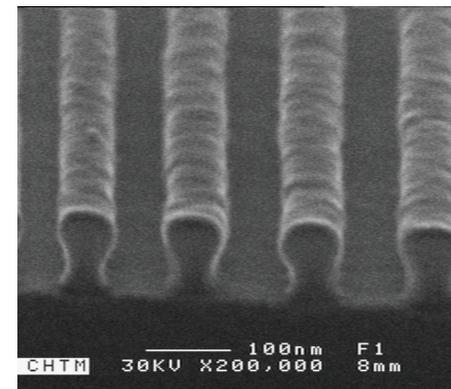
# NANOSTRUCTURE ENGINEERING – ENABLING TECHNOLOGIES



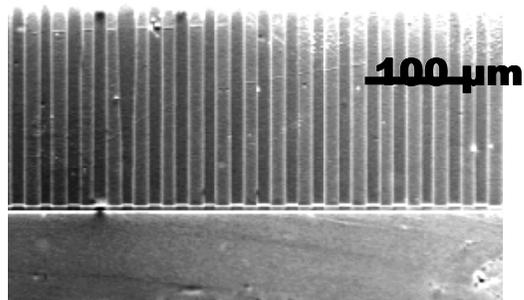
Quantum Dashes  
@ 1.67  $\mu\text{m}$



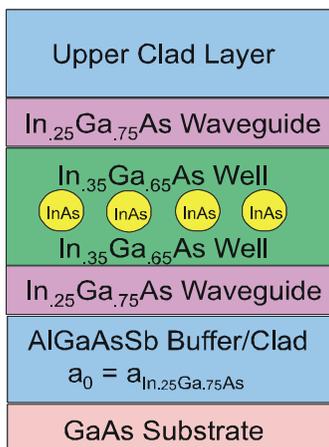
Quantum Dot  
Modeling



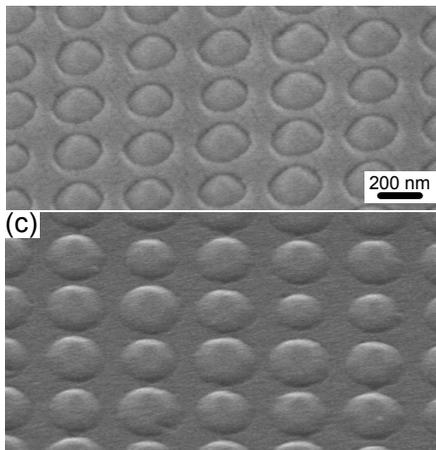
150-nm pitch, 50-nm CD  
lithography



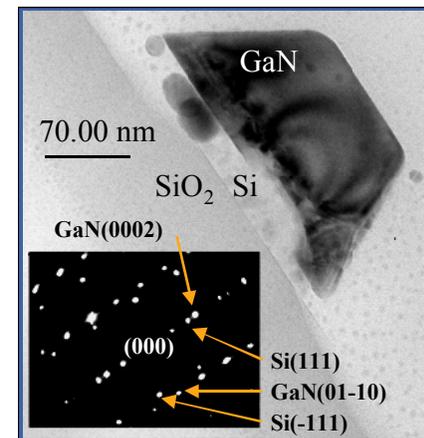
Orientation  
Patterned AlGaAs



Metamorphic  
Buffer



Nanopatterned Epitaxy



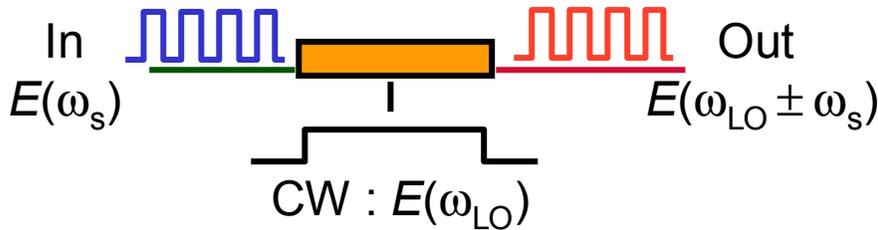
Nanoheteroepitaxy



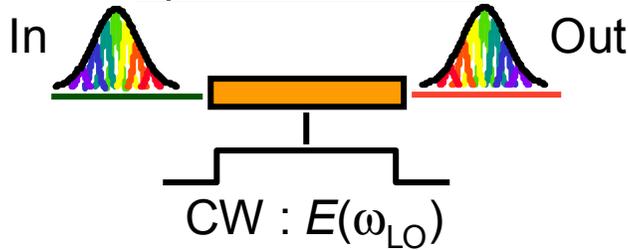
# OPTICAL FREQUENCY MIXERS FOR SIGNAL PROCESSING

- **Devices are very versatile**
- **>> 100 GHz modulation bandwidth**
- **> 50 dB dynamic range**
- **> 60 nm tuning bandwidth**
- **Transparent to data format**
- **Negligible additive noise**
- **~ 3.5 dB fiber-fiber insertion loss**

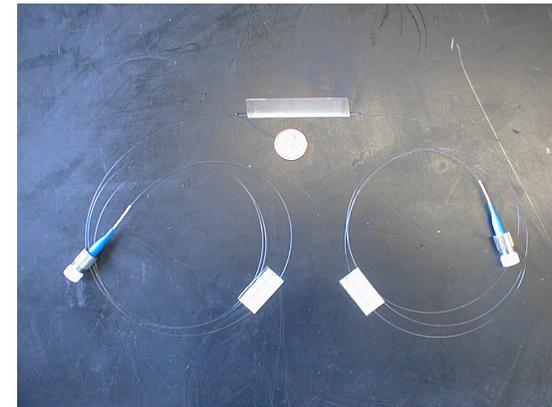
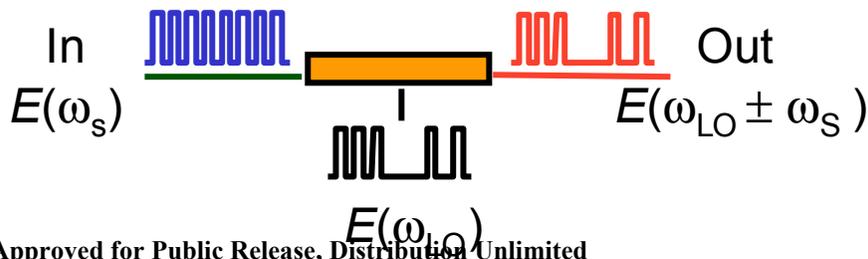
## Wavelength Converter



## Spectral Inverter



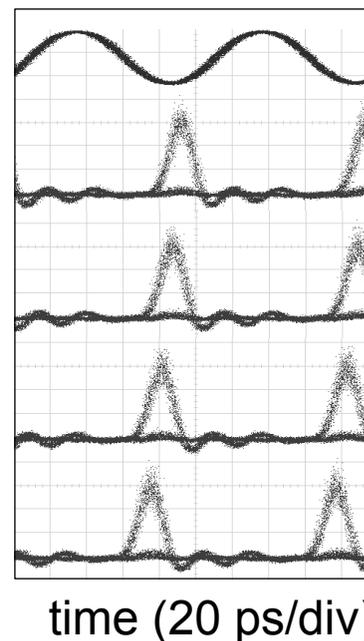
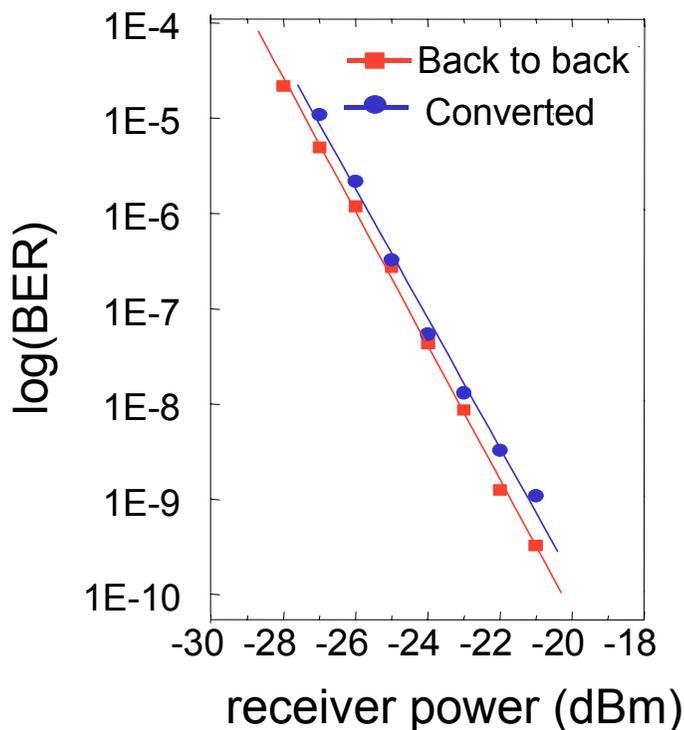
## Time Gated Mixer



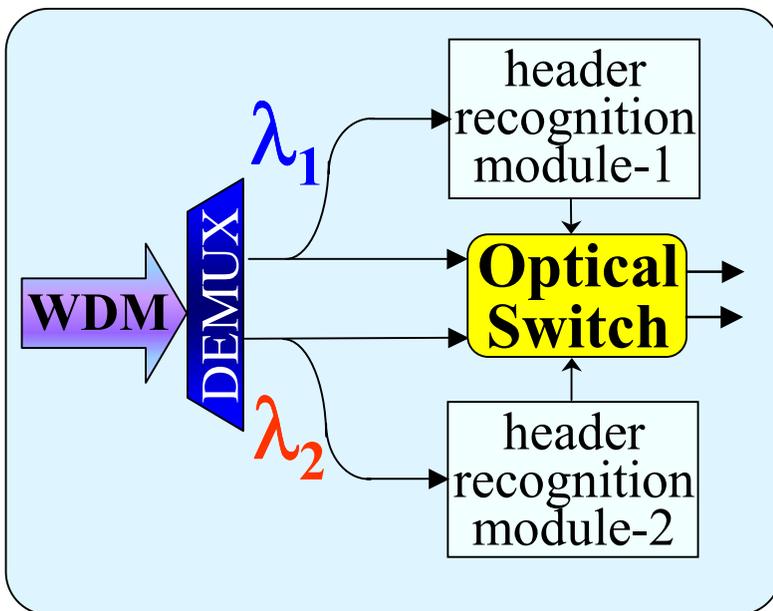


# DYNAMIC PERFORMANCE AT 160 GB/S

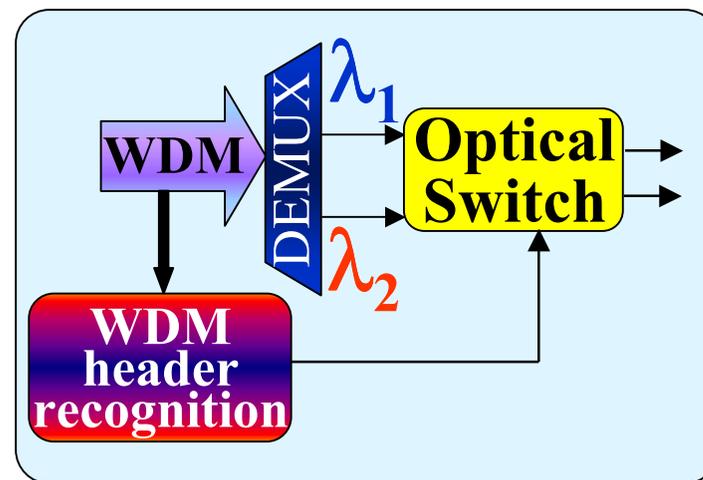
- Power penalty is very small
- Eye diagrams at receiver are very clean
- Theoretical speed > 1 THz (much faster than those possible with devices using carrier dynamics, such as SOAs)



# SINGLE AND MULTIPLE CHANNEL HEADER RECOGNITION (HR)



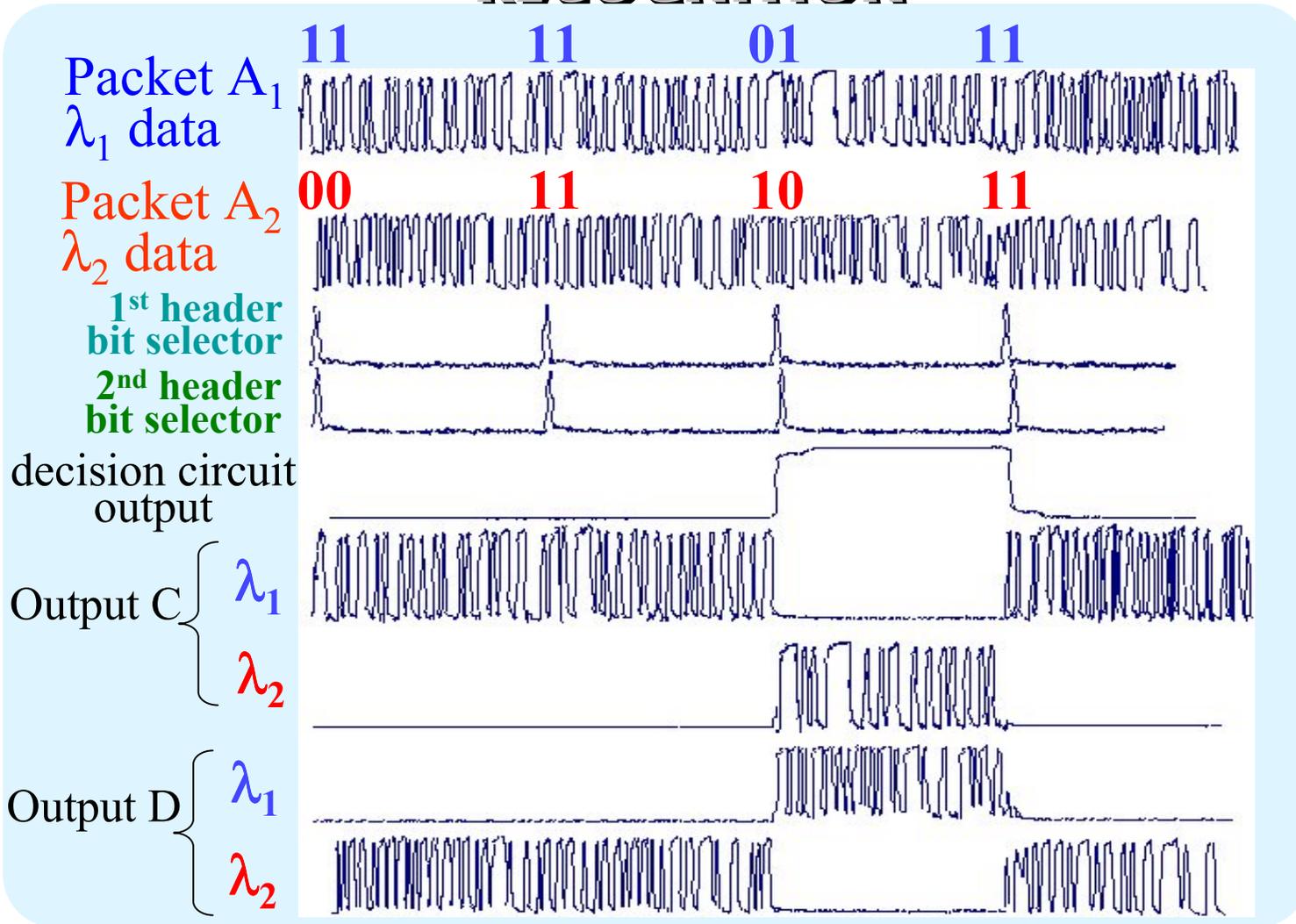
**Single channel HR**  
requires more components  
than WDM-HR



**Simultaneous all optical**  
header recognition of  
**multiple wavelengths**



# RESULTS OF MULTI-WAVELENGTH HEADER RECOGNITION





## **Commercial Interest and Future Work**

- **Several companies currently exploring commercial implementation of OF mixers**
- **Same family of mixer devices useful for a variety of applications (wavelength conversion, spectral inversion, dispersion compensation, gated mixing, optical signal processing, etc.)**
- **Develop MgO:LN for improved device stability (photorefractive resistance)**
- **Implement multi-channel wavelength converters with buried waveguide configuration for high efficiency**
- **Fabricate advanced integrated structures for higher functionality (balanced mixing, multiplexing, WDM broadcasting, all-optical switching)**



# ERROR RATES

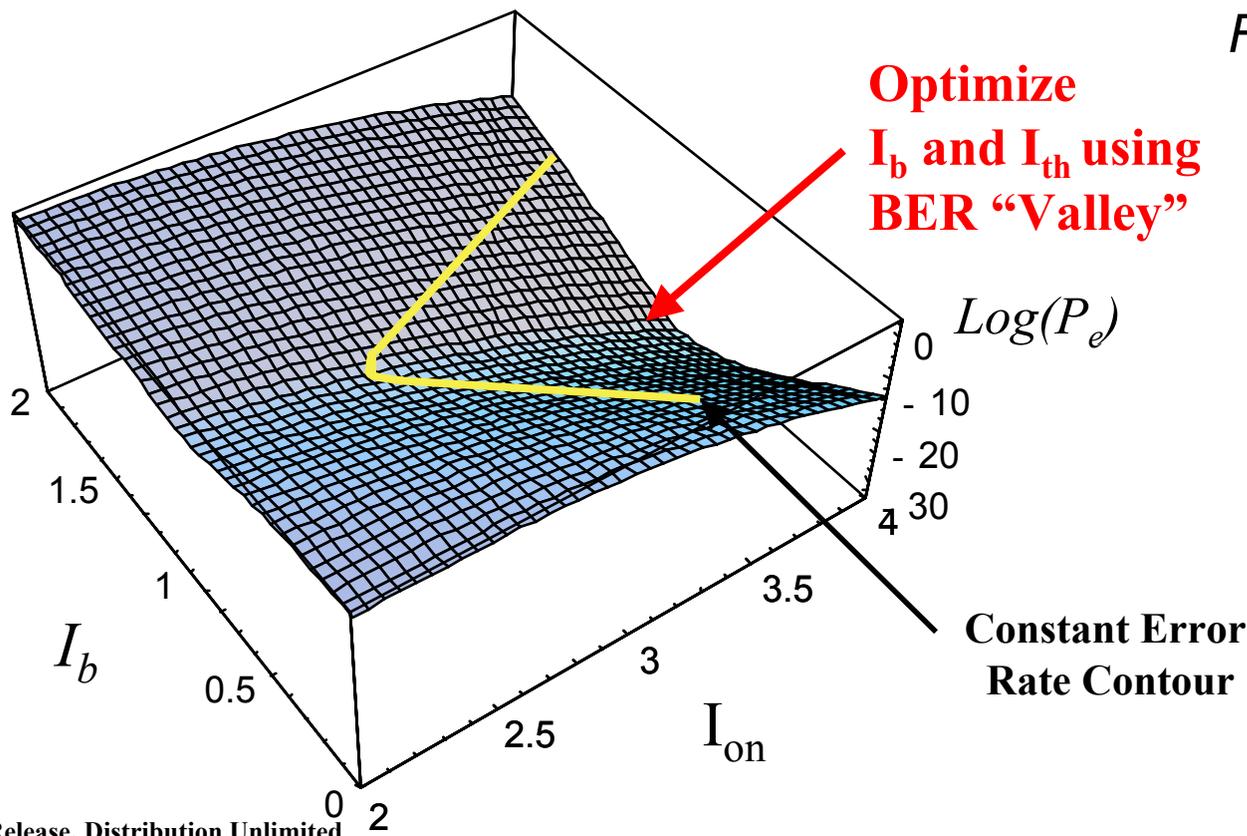
## Above Threshold

$$P_e = 0.5 \operatorname{Erfc} \left[ \frac{\gamma(I_{on} - I_b)}{\sqrt{2}} \right]$$

## Below Threshold

$$P_e = 0.5 \operatorname{Erfc} \left[ \frac{\gamma(I_{on} - I_{th}) \operatorname{Cos}(\pi B \tau F)}{\sqrt{2}} \right]$$

$$F = \operatorname{Ln} \left[ \frac{I_{on} - I_b}{I_{on} - I_{th}} \right]$$

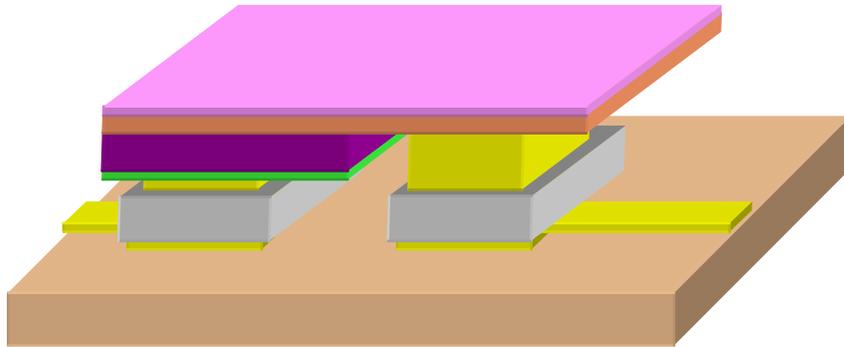


$Bt=1$
$I_{th}=1$
$g=4$



# OPTICAL INTERCONNECTS USING FLIP-CHIP BONDING

## GaAs modulator



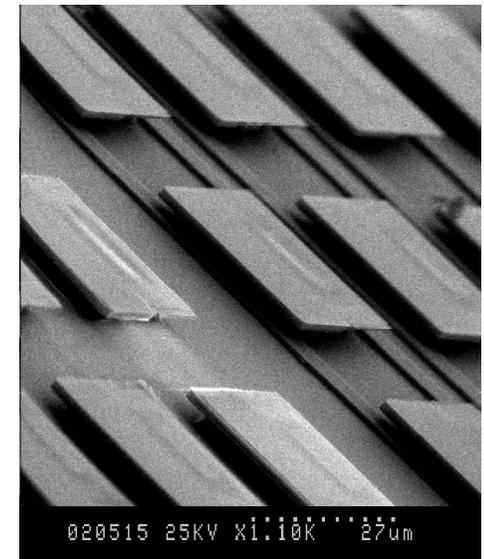
## Si CMOS

Flip-chip bonding enables *post-processing* integration of circuitry (Si CMOS) and optoelectronic devices (GaAs modulators and photodiodes)

- Mature CMOS process + optimized optoelectronics.
- Dense 2D arrays bonded in parallel with high yield.
- Lower noise and higher speeds due to reduced total capacitance.

- Successful applications of flip-chip bonding to CMOS
  - Demonstration of optical link in both WDM and short pulse modes.
  - First measurement of the latency of an optical interconnect Tx/Rx pair.
  - Novel single-ended receiver design operating at 1.6 Gb/s.
  - Experiment showing removal of signal skew and jitter.

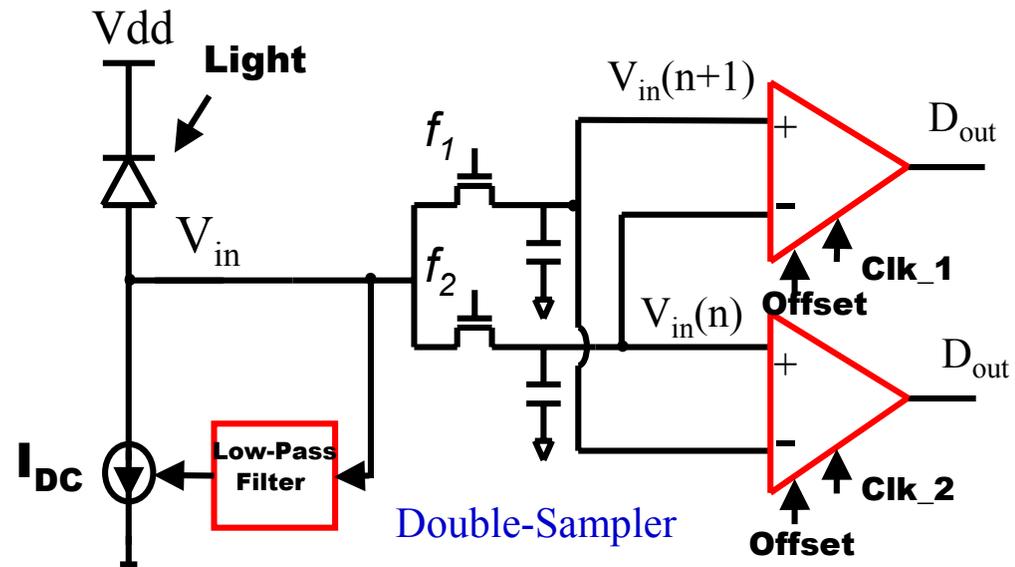
D Miller and M  
Horowitz





# A 1.6 GB/S, 3mW CMOS OPTICAL RECEIVER WITH FLIP-CHIP BONDED OPTICAL DEVICES

- Traditional designs use a Transimpedance Amp.
  - Requires high gain-bandwidth, which means high power, exotic technology
- New Low-Power Design
  - Integrates photo current into the parasitic input capacitor
  - Samples the voltage of the input node at two consecutive bit times
  - Compares these two values with the following clocked Sense Amp
  - Adjusts input bias voltage, AC couples the input with a simple feedback loop
- Lower Power, Smaller Area, Comparable Bandwidth and Sensitivity

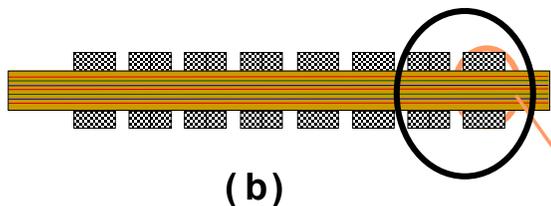


Clocked Comparators  
with Offset Compensation

M Horowitz  
and D Miller

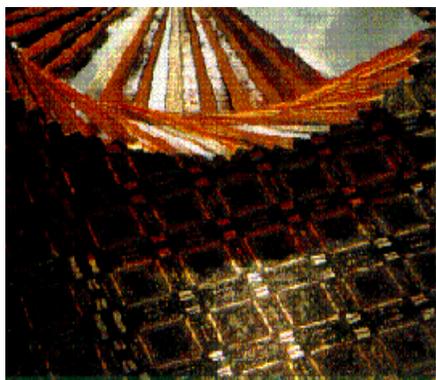


# SCHEMATIC OF EMBEDDED OPTOELECTRONIC INTERCONNECTS

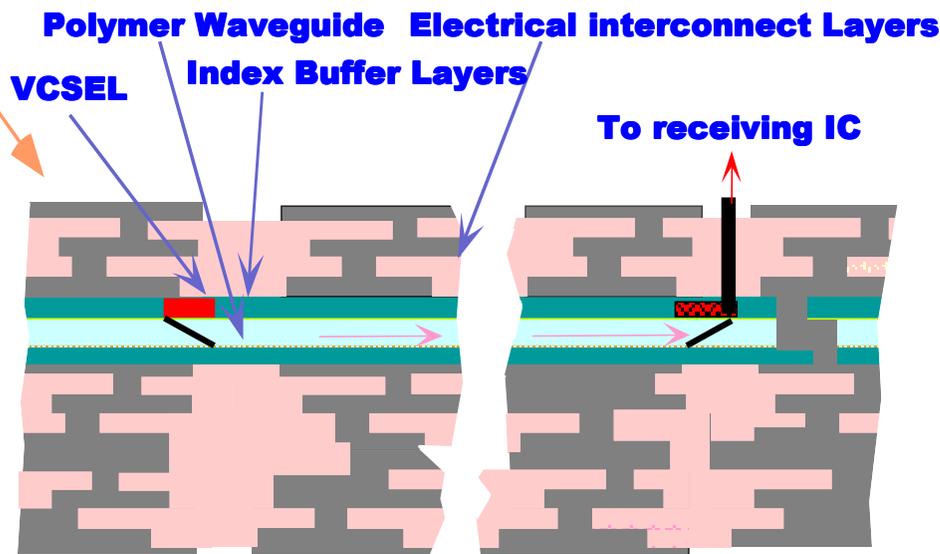


(b)

-  **Thin-film VCSEL (Vertical cavity surface emitting laser)**
-  **Polymer Waveguide**
-  **Si Photodetector**
-  **Interlayer Dielectric**
-  **Waveguide Coupler**
-  **Electrical Interconnects**



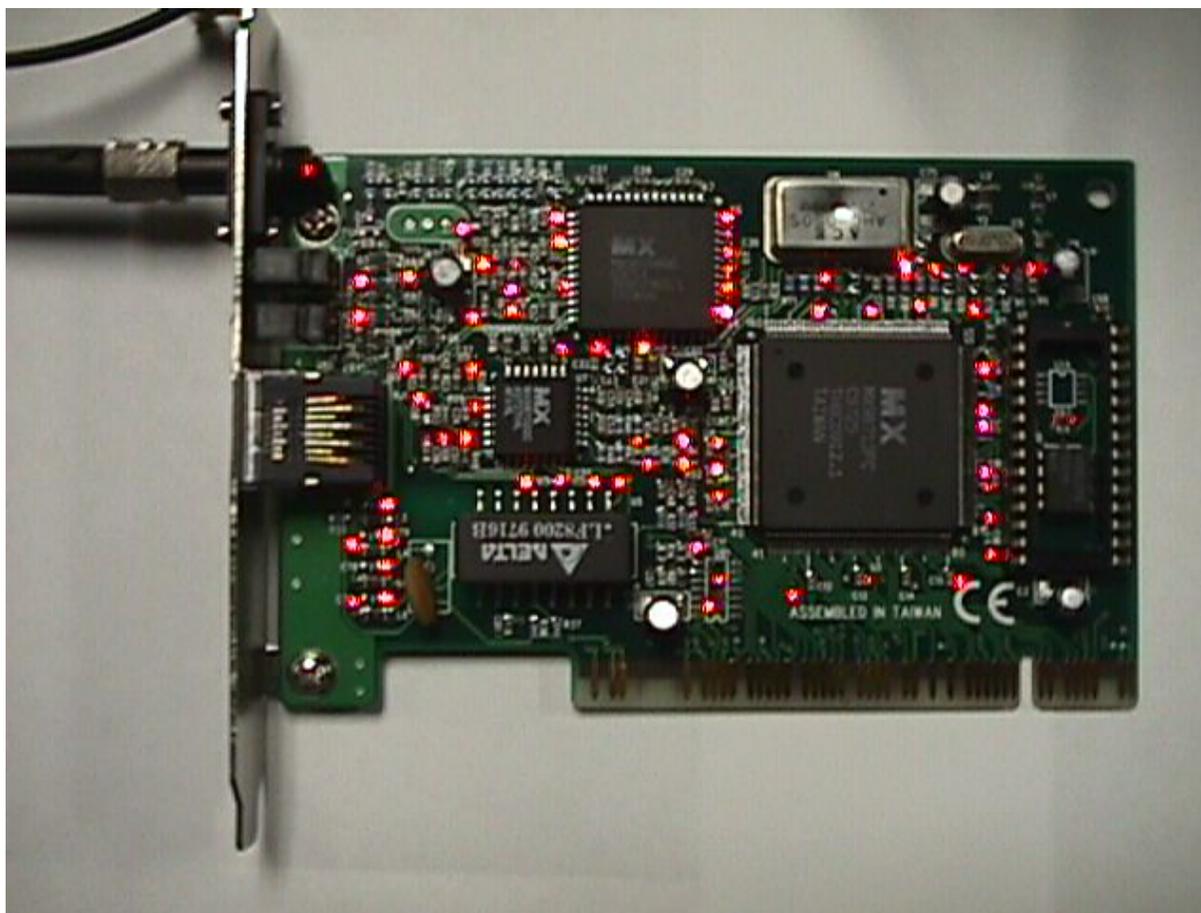
(a)



Section of Electrical/Optical Interconnects on a multilayer Board



# OPTICAL SIGNAL DISTRIBUTION IN A NETWORK CARD



R. T. Chen

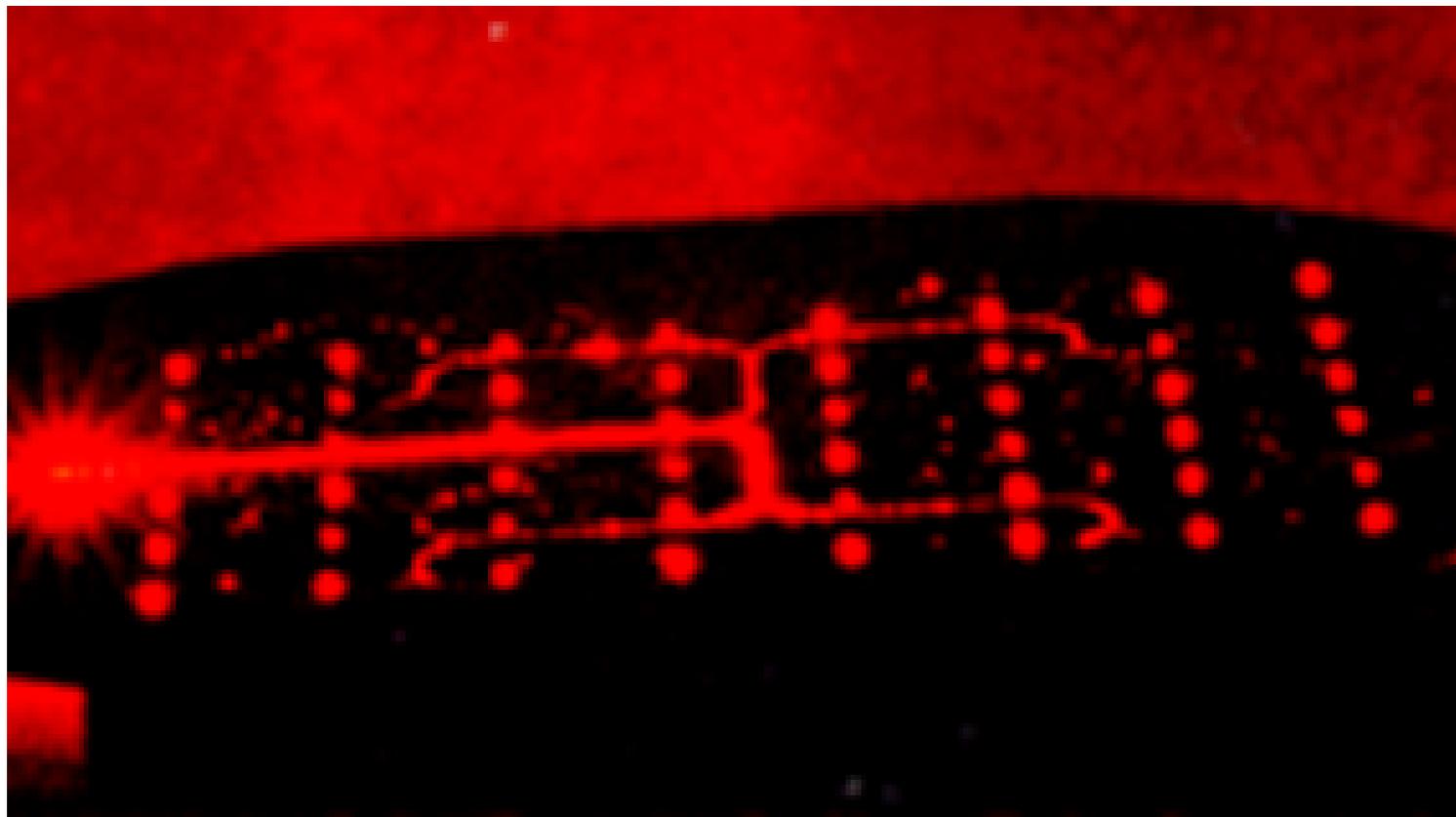


High Capacity  
Optoelectronic  
Interconnects

UNIVERSITY OF NEW MEXICO  
STANFORD UNIVERSITY  
UNIVERSITY OF ILLINOIS  
UNIVERSITY OF TEXAS - AUSTIN  
UNIVERSITY OF SOUTHERN CALIFORNIA



# POLYIMIDE BASED 1-TO-48 FANOUT H-TREE OPTICAL WAVEGUIDE ON SI-SUBSTRATE

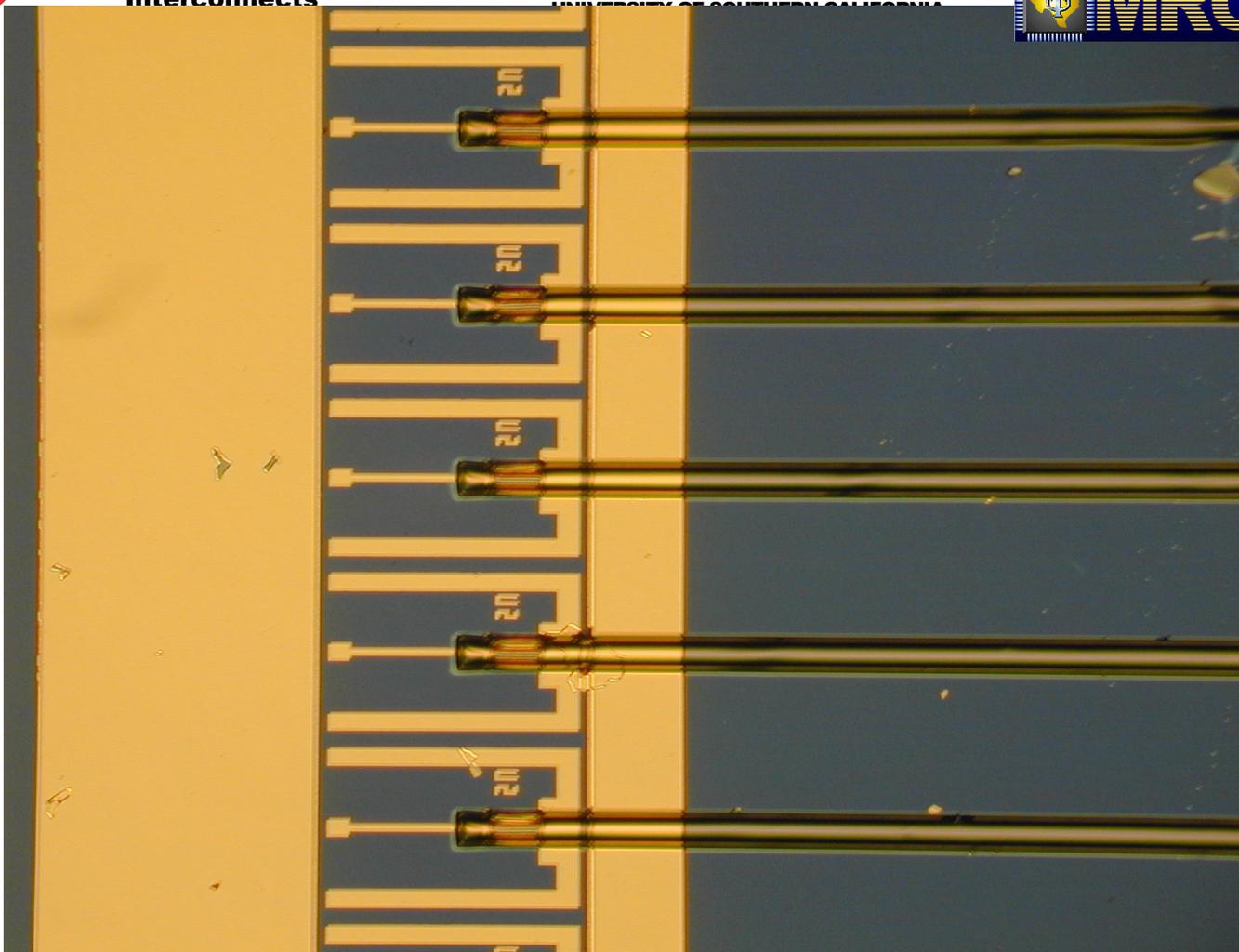


R. T. Chen



**High Capacity  
Optoelectronic  
Interconnects**

UNIVERSITY OF NEW MEXICO  
STANFORD UNIVERSITY  
UNIVERSITY OF ILLINOIS  
UNIVERSITY OF TEXAS - AUSTIN



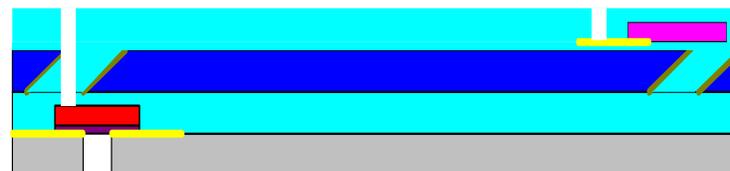
**R. T. Chen**



# INTEGRATION ON PWB



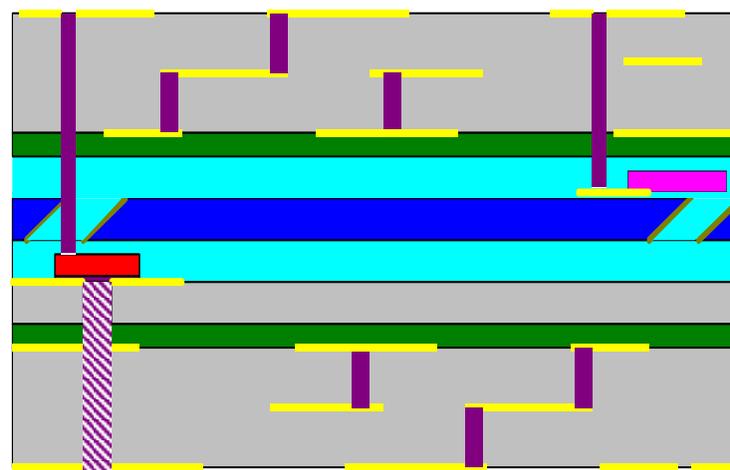
(a)



(e)



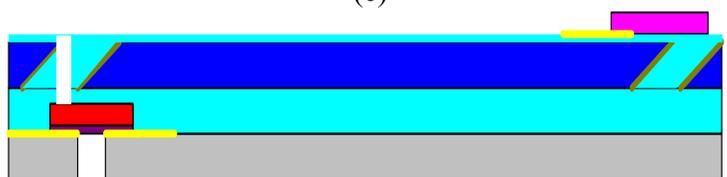
(b)



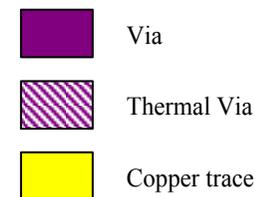
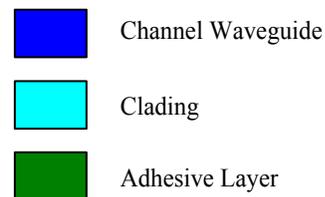
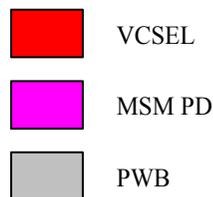
(f)



(c)



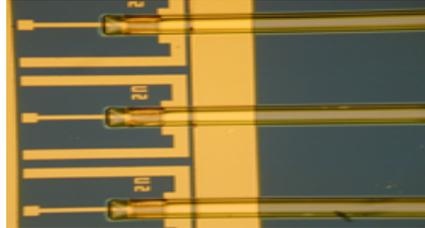
(d)





## SUMMARY

1. Demonstration of Channel waveguide formation with micro-mirror
2. Integration of MSM detector array with waveguide array



R. T. Chen

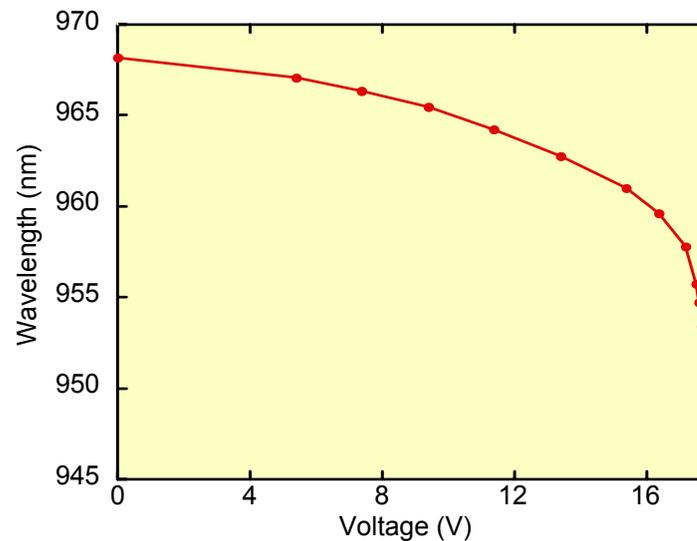
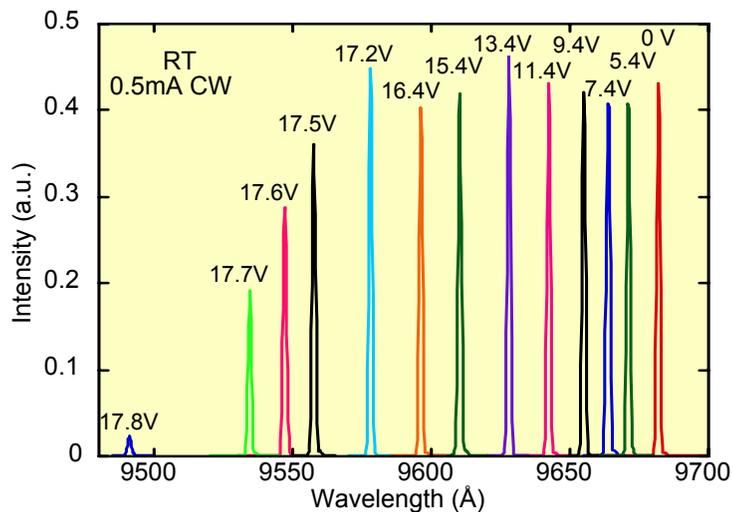
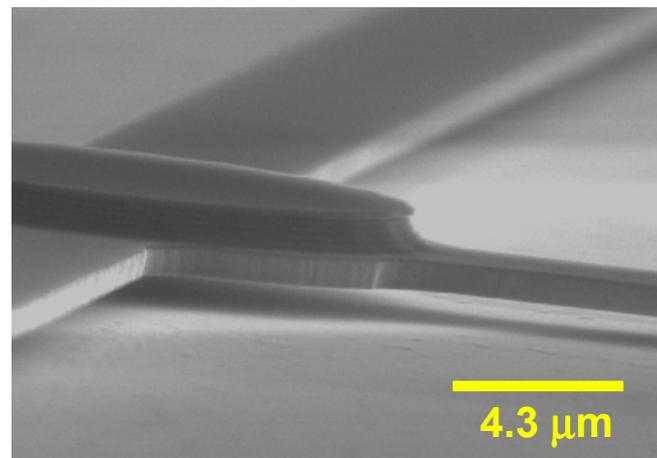
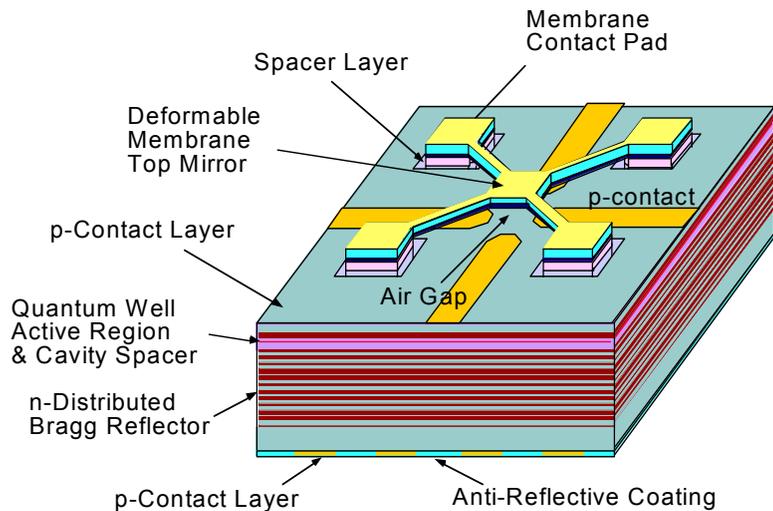
### 3. Study of thinning process of commercial VCSELs

#### 4. Point to point interconnect demonstration

- Reference junction temperature ( $q_{jc}$ ) = 44.4 °C ( block Cu heat sink @ 25°C)
- 250µm thick Cu heat sink can not be used because of difficulty to form (not standard PWB process).
- 30 µm thick electroplated Cu heat sink is preferable because it is standard process for through hole plating.
- Thermal resistance should be less than 1080 K/W to operate up to 85 °C environment.
- Maximum thickness of VCSEL to satisfy thermal budget is 150µm for 30µm thick electroplated Cu heat sink.
- Very thin VCSEL shows good performance, however process is difficult and expensive.



# Tunable Micromachined VCSELs

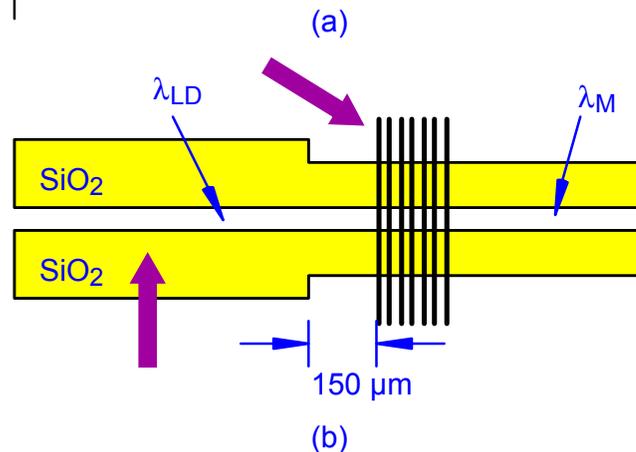
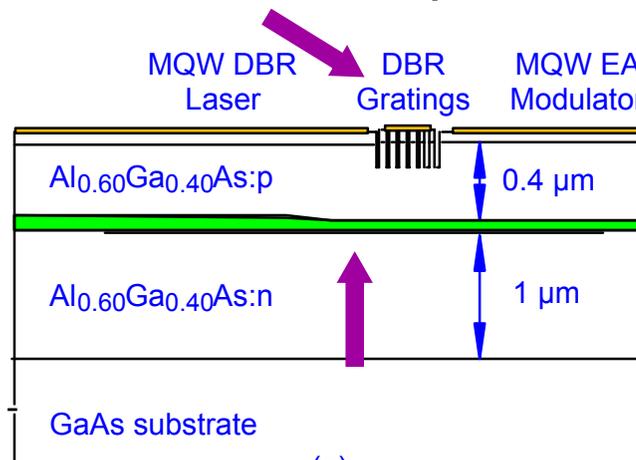


# SELECTIVE AREA EPITAXY FOR INTEGRATED LASER/MODULATOR MODULES

## Approach

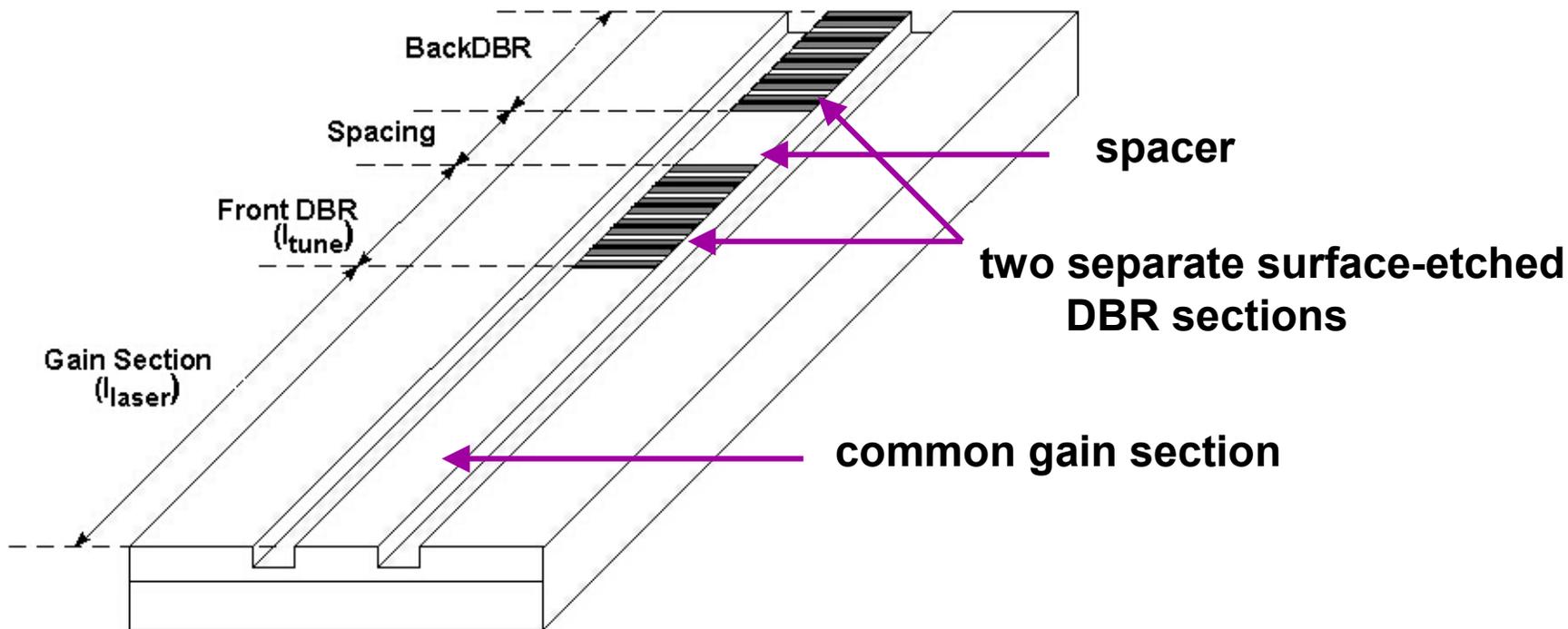
- Selective-area MOCVD growth of engineered bandgap structures using a patterned oxide mask
- DBR diode laser master oscillator, slightly blue-shifted electroabsorption modulators, heavily blue-shifted (transparent) splitter and router waveguides
- Extension to quantum dots for performance and wavelength considerations

Selective-area epitaxy (SAE) tunable narrow linewidth laser/electro-absorption modulator



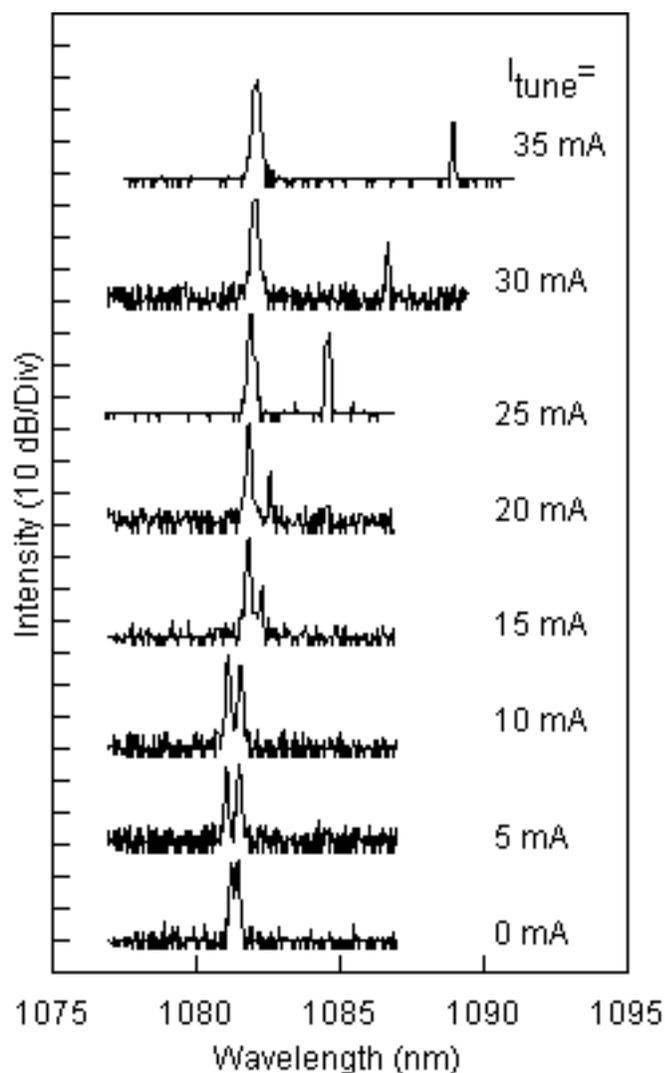
SAE oxide mask pattern

# Dual-Wavelength Ridge Waveguide DBR Lasers with Tunable Mode Separation

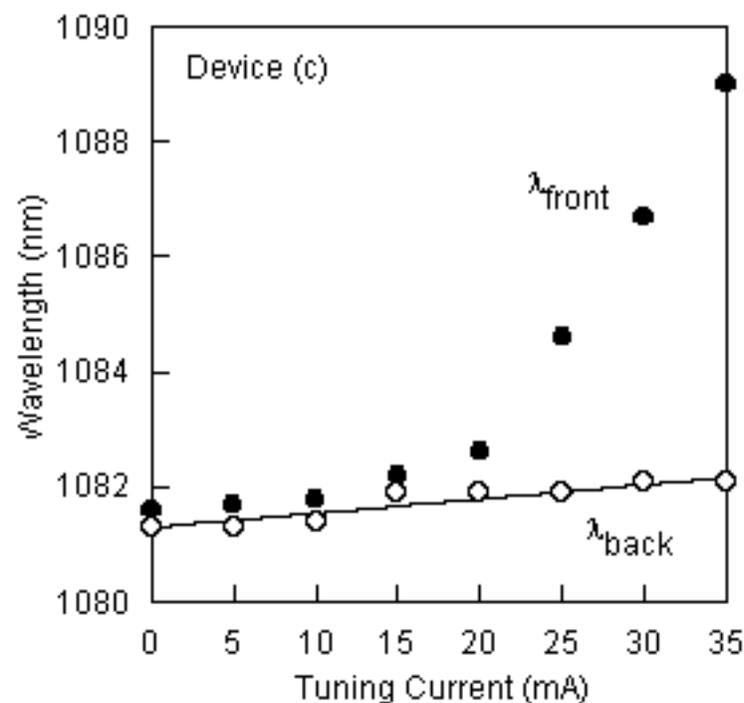


Relatively low coupling coefficient  $k$ , in the front grating reduces the added cavity loss for the back grating mode

Biassing the front DBR section results in tunable mode pair separations ( $\Delta\lambda$ ) as small as 0.3 nm and as large as 6.9 nm

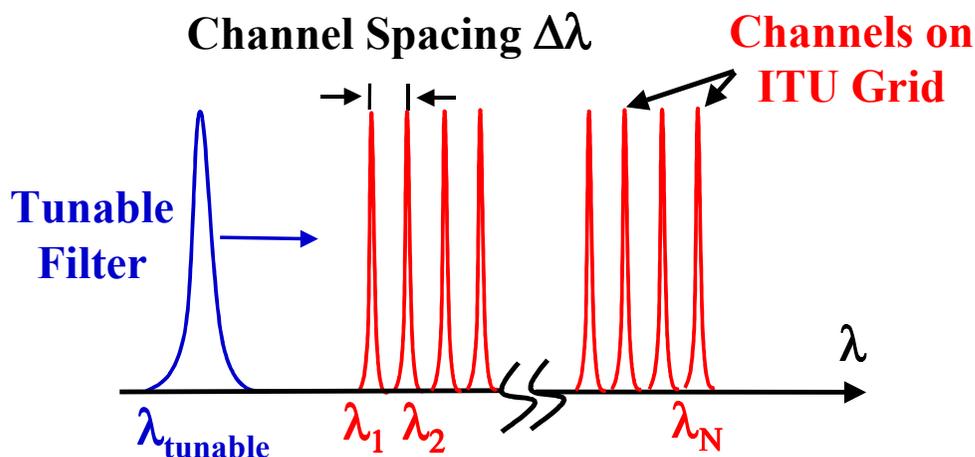


## Spectra as a function of front DBR grating tuning current ( $I_{\text{tune}}$ )



The spacer reduces inadvertent drift in the back DBR grating

# Wavelength-Agile Sources: Concept & Results



## WDM Source: Principle of Operation

- Intracavity multi- $\lambda$  **grid filter** provides precise feedback at ITU-WDM channels
- Intracavity **tunable filter** selects individual wavelength channels

## Choices of Multiwavelength Glass Waveguide Grid Filters (MWGFs)

- Series of WBGs (FBGs) / Sampled WBGs (FBGs)
- Waveguide (Fiber) Fabry-Perot Filters
- All-Waveguide “Sagnac Loop” Filter

R. Jain

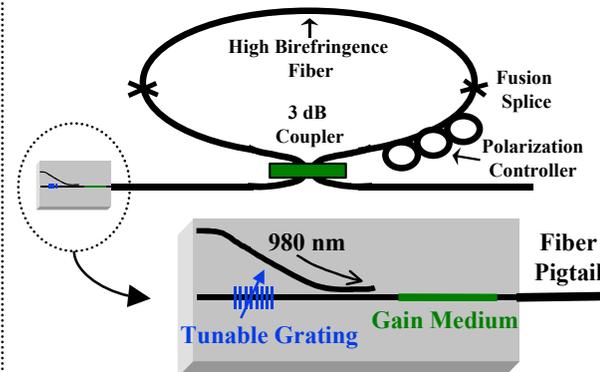
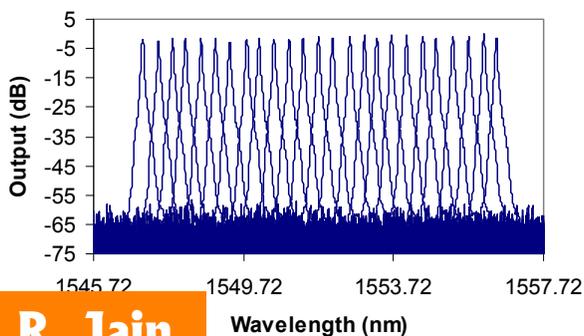
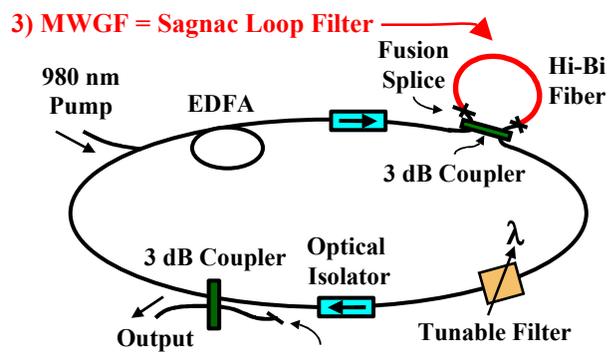
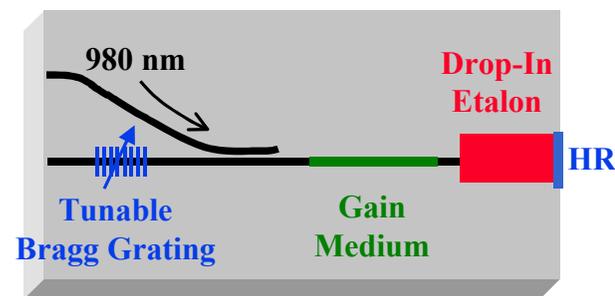
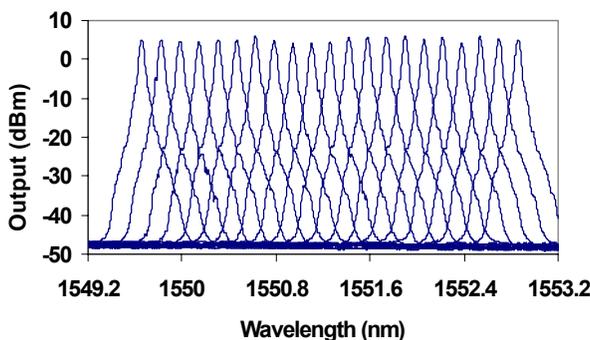
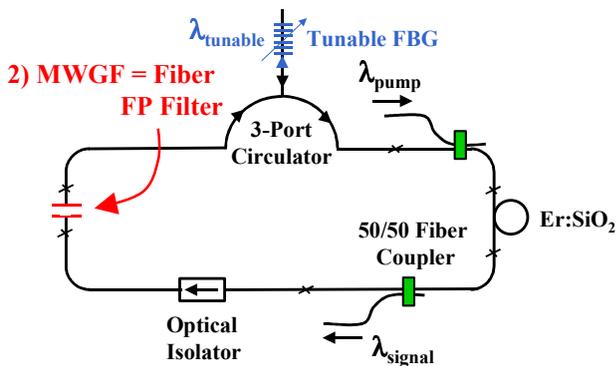
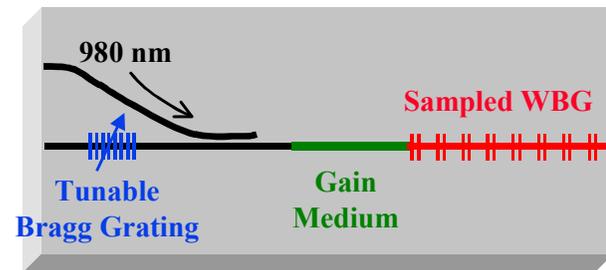
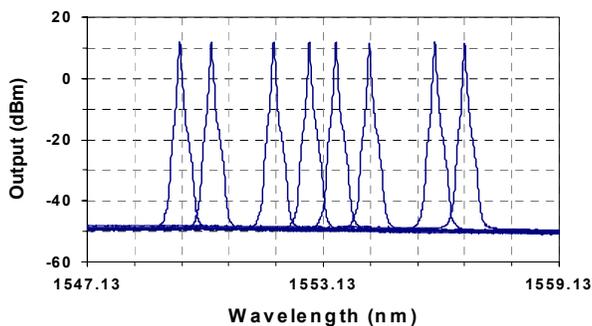
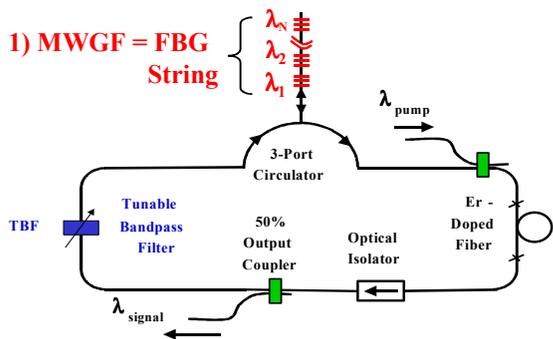


# FIBER WDM SOURCES & FUTURE PLC IMPLEMENTATIONS

## Fiber Laser Designs

## Results

## Future PLC Designs



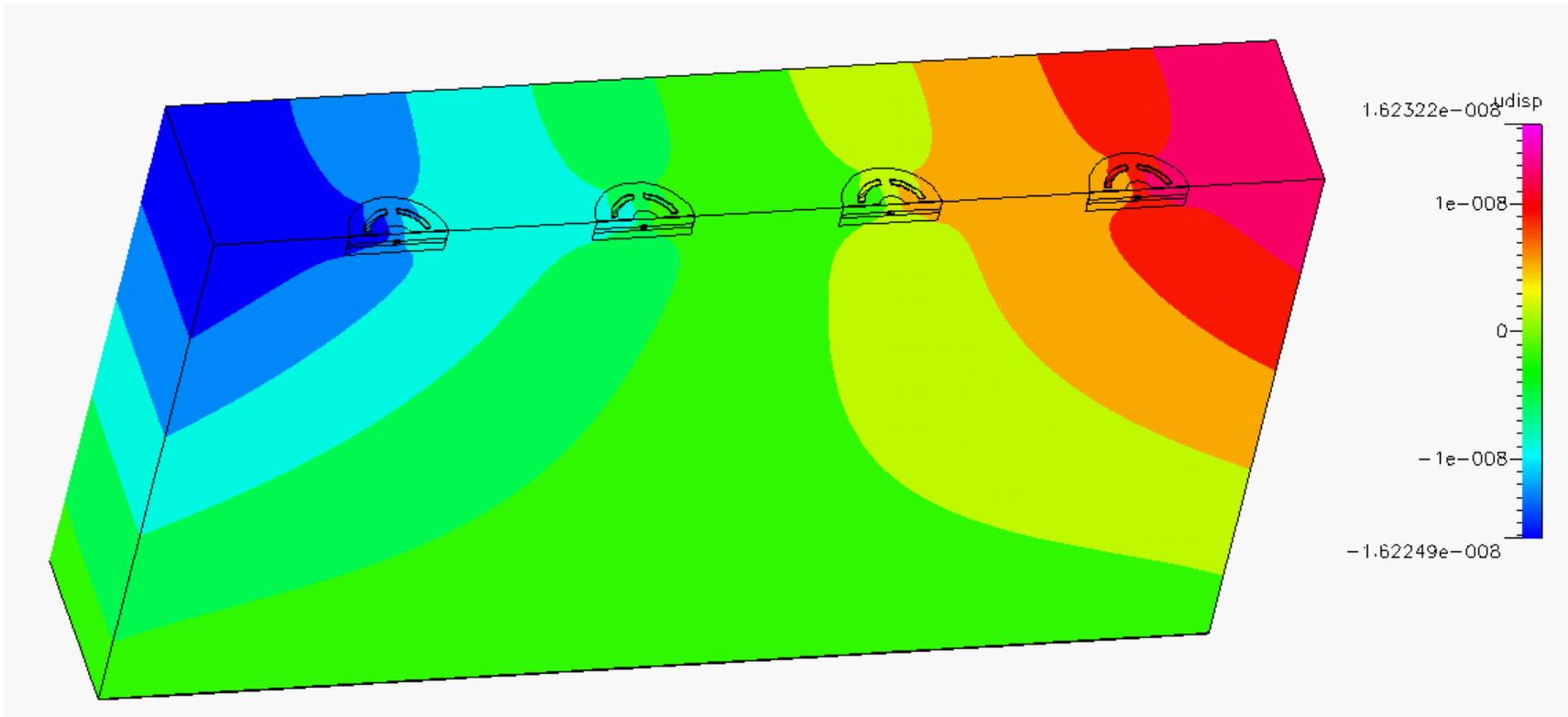


## VCSEL SIMULATION GOALS

- Develop self-consistent 3D electrical-thermal-optical simulator suitable for VCSEL design and analysis
- Explore complex physics of ETO interactions in cw-operating VCSELs and 2D VCSEL arrays
- Apply the new tools to design novel VCSEL structures and to improve performance of existing devices
- Develop reduced equivalent circuit versions for multi-level simulation

# PACKAGE-LEVEL SIMULATION OF VCSEL ARRAYS

Results of 3D electro-thermo-mechanical simulation  
- Deformation and VCSEL displacement



Max. displacement of 4 VCSELs:  $0.032 \mu\text{m}$  - for 36 VCSELs:  $0.3 \mu\text{m}$  !

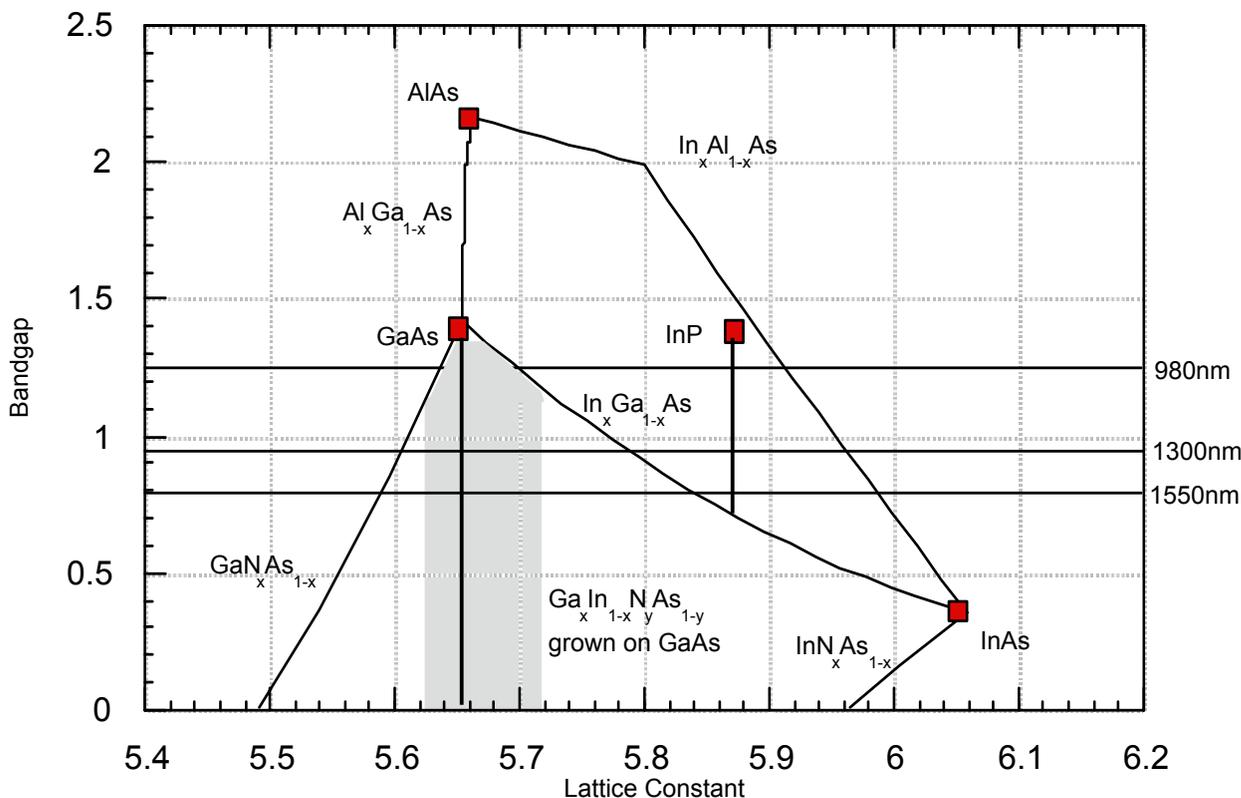
M. Osinski



CFDRC



# GalnNAs, a Long Wavelength, Low Voltage Material for Optical Interconnects



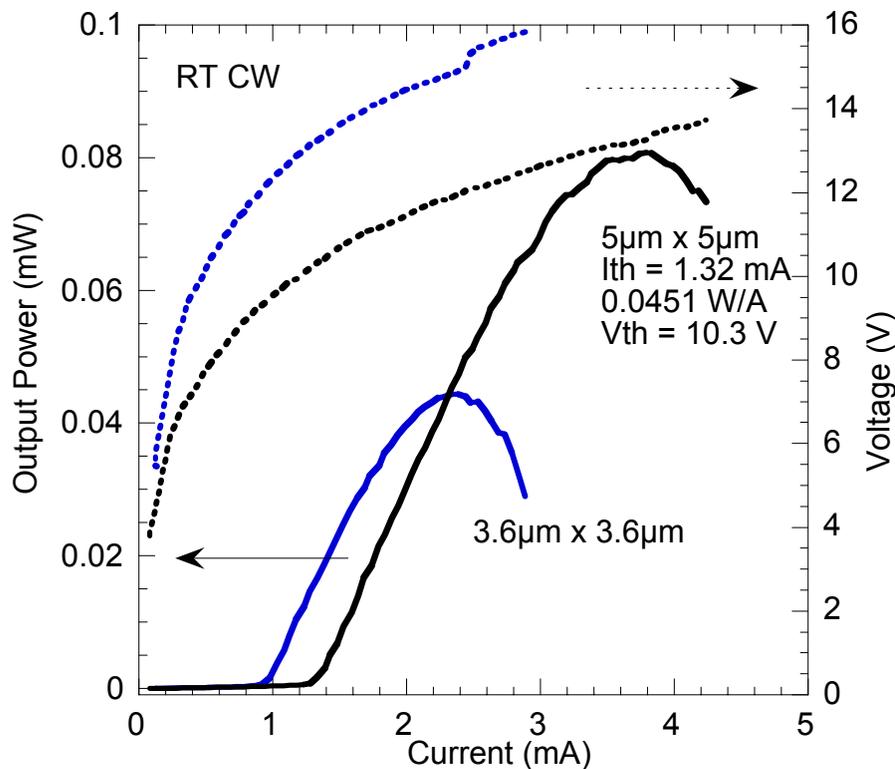
- Scaled CMOS compatible ( $< 1V$ )
- Si substrate transparent
- Applicable to modulators, VCSELs and detectors
- Compatible with telecommunications wavelengths

J. S. Harris

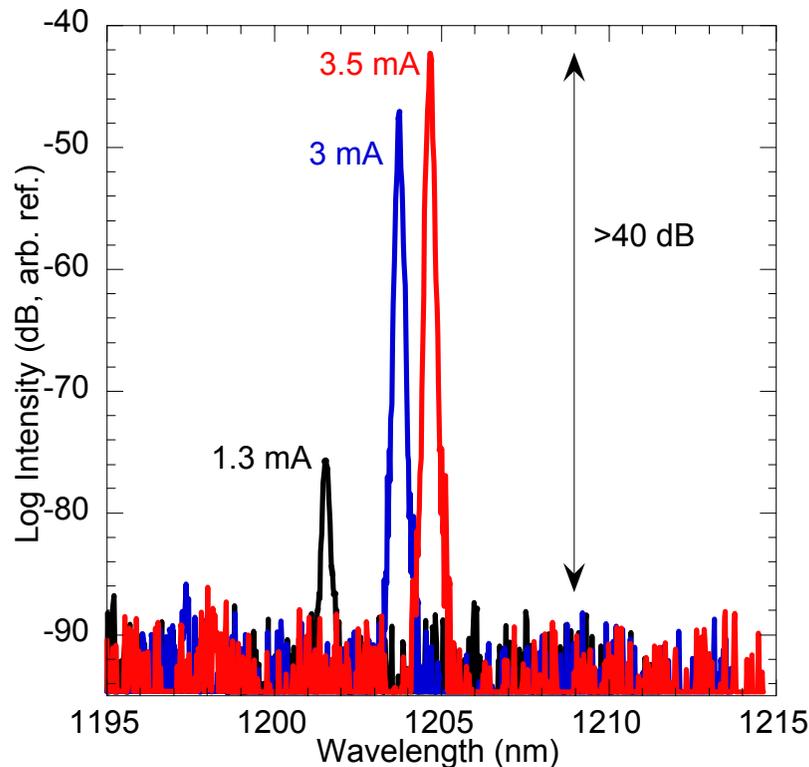


# GaN NAs VCSEL Room Temperature CW Operation

## Output Power vs Current



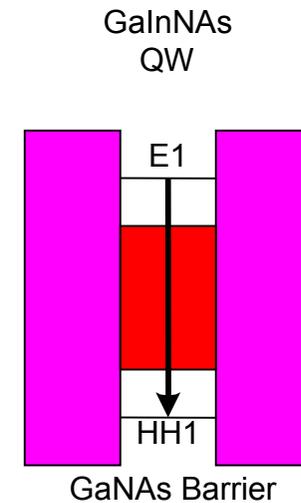
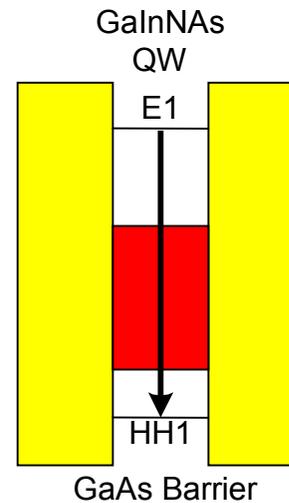
## Spectra (5 $\mu$ m x 5 $\mu$ m)



- 5 $\mu$ m aperture: 1.3 mA threshold; 3.6 $\mu$ m: < 1 mA
- CW operation in spite of very high voltage drop ( $\sim 9$ V) in top mirror

# Advantages of GaNAs Barriers

- Decreased carrier confinement
- Emission at longer wavelengths

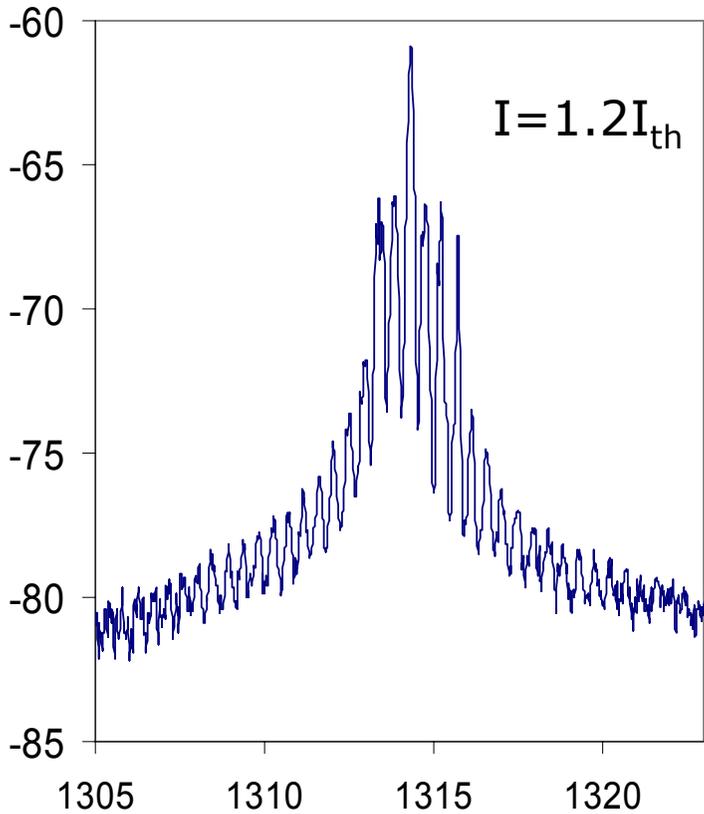


- Decreased Nitrogen out-diffusion during anneal → lower emission blueshift
- Strain compensation possible
  - GaAsN - tensile
  - GaInNAs - compressive

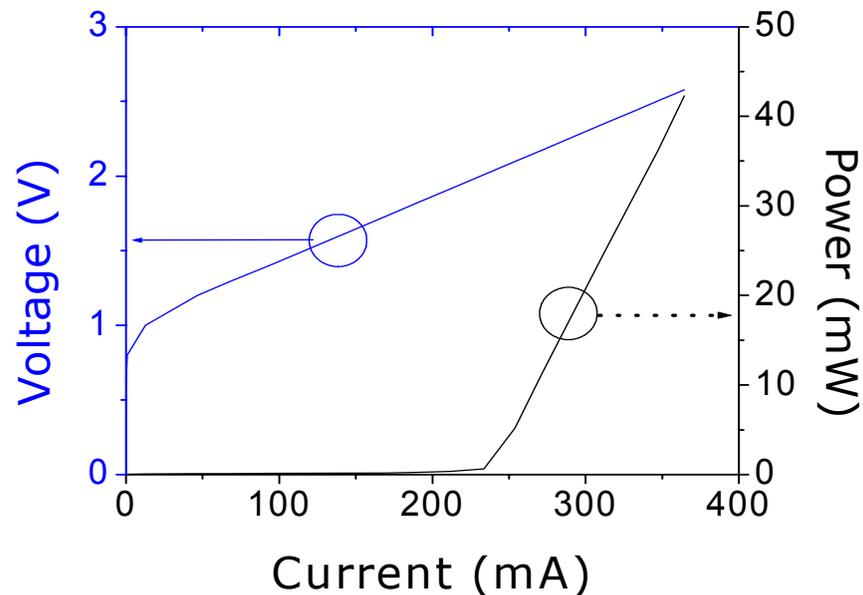


# Ridge-Waveguide Laser Diode Results

### Optical Spectrum



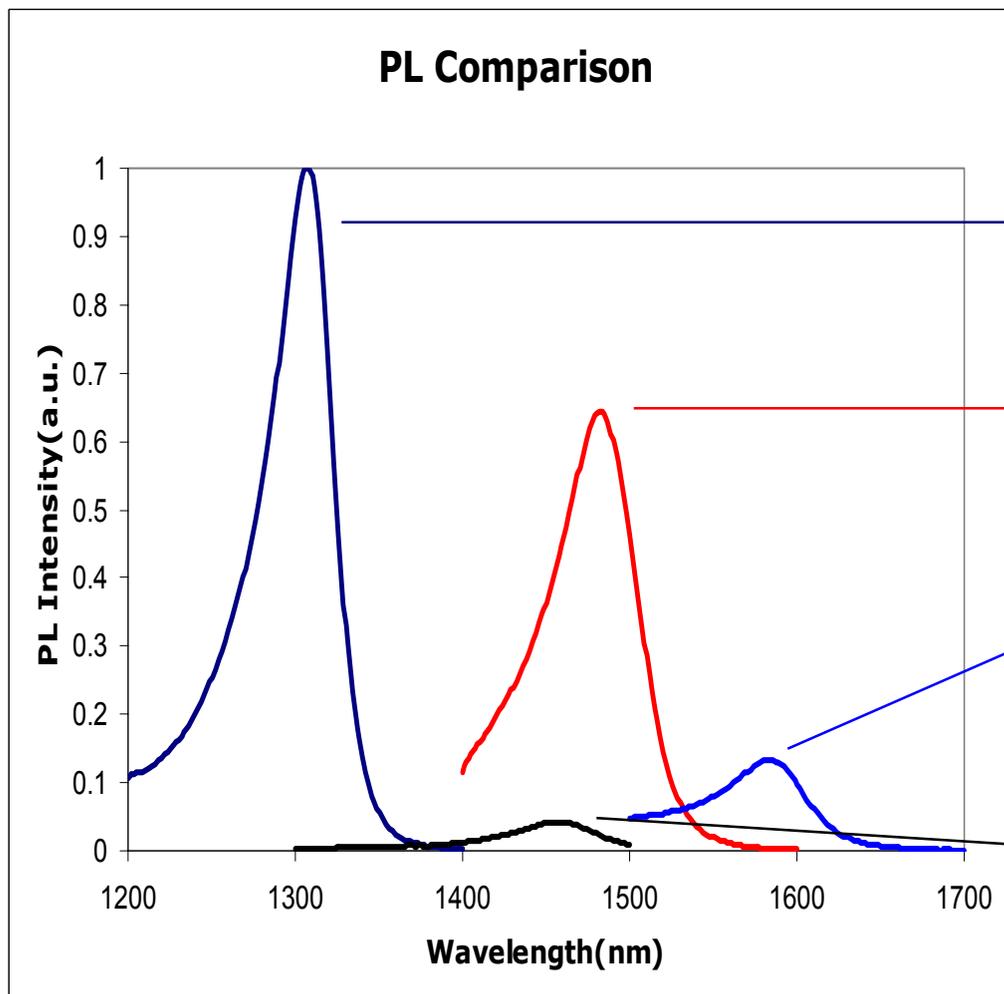
Wavelength(nm)



- $Ga_{0.68}In_{0.32}N_{0.025}As_{0.0975}$  with  $GaAs_{0.965}N_{0.035}$  barriers
- Emission spectrum at  $1.315\mu m$
- Without AR/HR coating



# GaInNAs(Sb)/GaNAs(Sb) PL Data



1.3μm Highest PL intensity

45% In, Sb flux 7.2E-8  
Peak at 1.482μm (0.65)

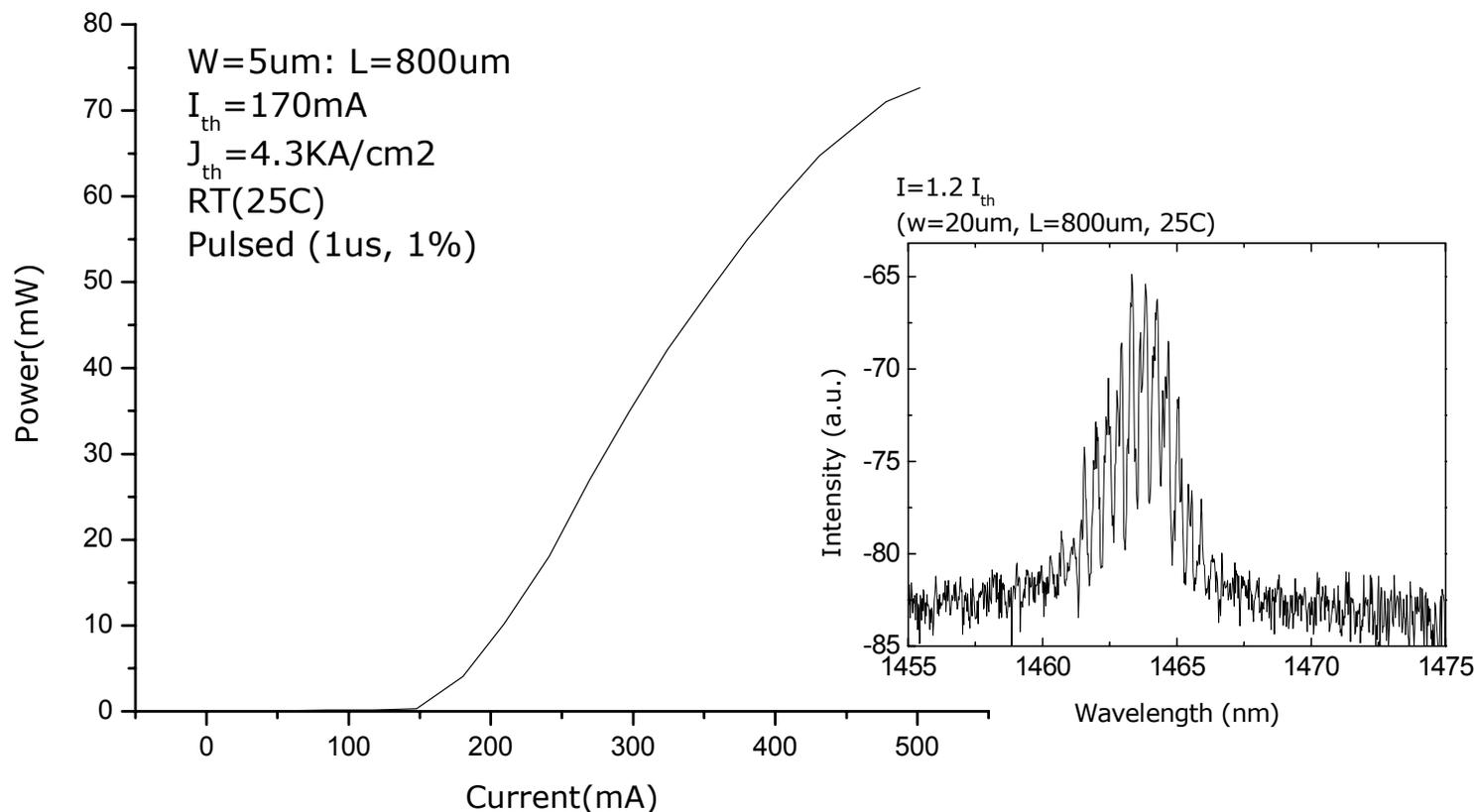
46% In, Sb flux 1.4E-7  
Peak at 1.584μm (0.14)

44% In, Sb flux 4.6E-8  
Peak at 1.458μm (0.043)

J. S. Harris



# GaNAsSb/GaNAsSbRidge Waveguide Laser



- $\text{Ga}_{0.56}\text{In}_{0.44}\text{NAs}(\text{Sb})$  quantum wells with  $\text{GaNAs}(\text{Sb})$  barriers

J. S. Harris



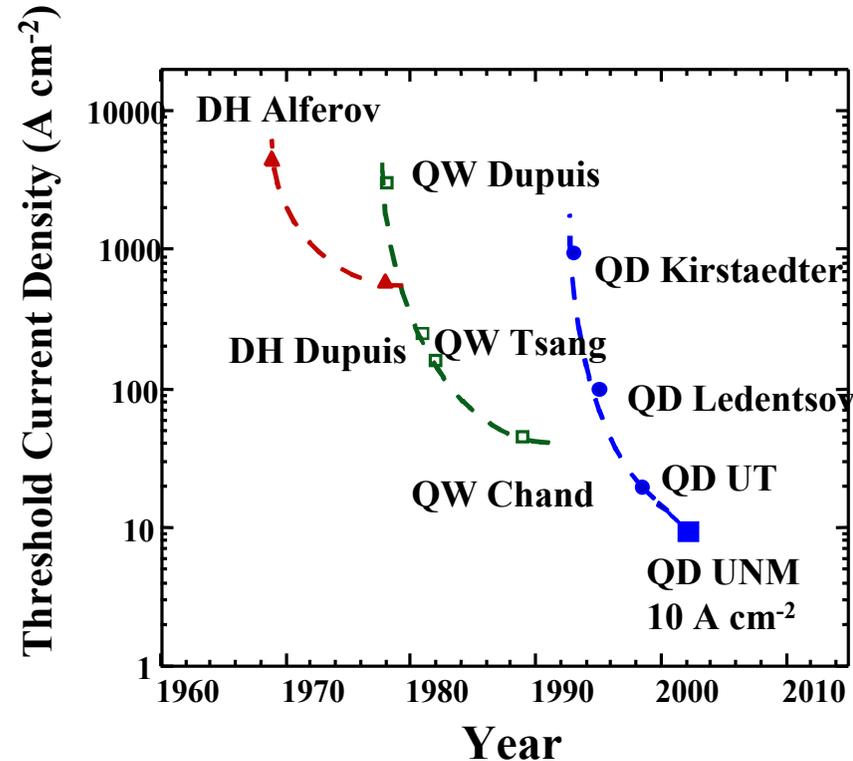
# GalnNAs HIGHLIGHTS

- Demonstrated first cw, room temperature GalnNAs VCSEL at  $1.22\mu\text{m}$
- Developed novel GaNAs barrier, GalnNAs quantum well structure for  $> 1.3\mu\text{m}$  lasers
- Developed optimum annealing process to achieve emission in  $1.3\text{-}1.4\mu\text{m}$  with low threshold currents ( $1.5$  and  $2.1\text{KA}/\text{cm}^2$ )
- Fabricated high efficiency ( $0.67\text{W}/\text{A}$ ),  $1.4\mu\text{m}$  ridge-waveguide lasers
  - High output powers exceeding  $320\text{mW}$
  - Device operation up to  $90^\circ\text{C}$
- PL extended to  $1.6\mu\text{m}$  by addition of Sb GalnNAs(Sb)



# OMC- World Leaders in QD Devices

- Lowest threshold current for any semiconductor laser diode -  $10 \text{ A cm}^{-2}$ 
  - DQ efficiency  $> 90\%$
- First quantum dot laser at  $1.3 \mu\text{m}$
- First quantum dot VCSEL
- First measurement of linewidth enhancement factor
  - QD lasers have less chirp during modulation, will have less noise, be less sensitive to feedback and resistant to filamentation
- Demonstration of  $200+$  nm tuning
  - 1.5 to  $1.3 \mu\text{m}$  in a single device?
- First mode-locked device
- Dots-in-a-well rapidly copied



K. J. Malloy  
L. Lester  
D. Huffaker



D. Deppe



J. J. Coleman

# Where is OMC going with QDs?

## ■ Commercialization

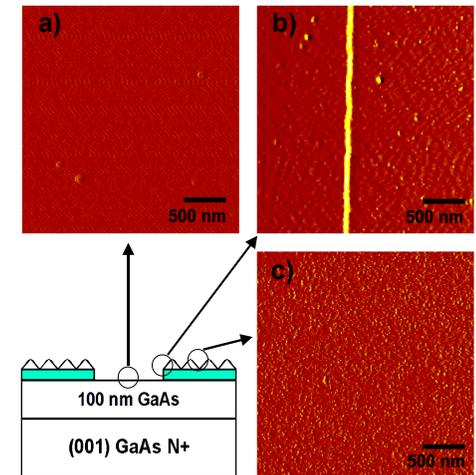
- Zia Laser, \$6M funding 1 June 2001
- Quantum dash lasers operating at 1.5 to 1.7  $\mu\text{m}$  on InP

## ■ 1.3 $\mu\text{m}$ VCSELs investigated

## ■ Long wavelength on GaAs

## ■ Modulators and amplifiers

## ■ MOCVD dots show potential



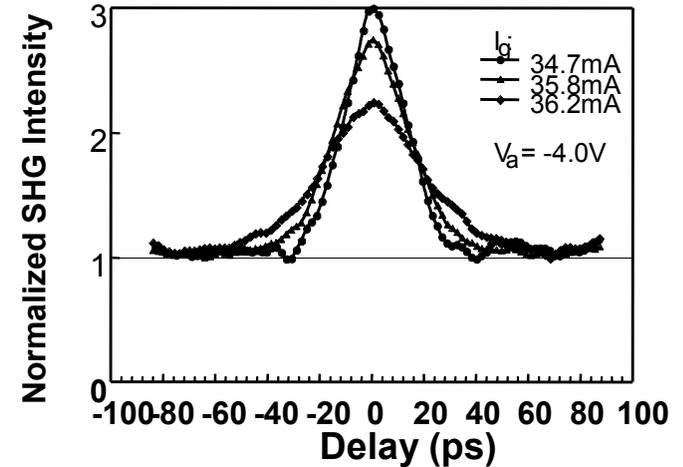
Selective MOCVD Dots

# NO PHONON BOTTLENECK IN QD DWELL LASERS

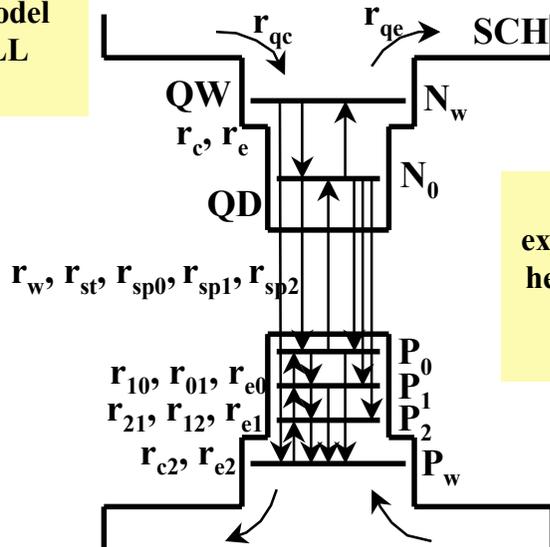
Modeling and experiment suggest capture occurs in QDs in less than 10 ps at room temperature:

Differential quantum efficiency high

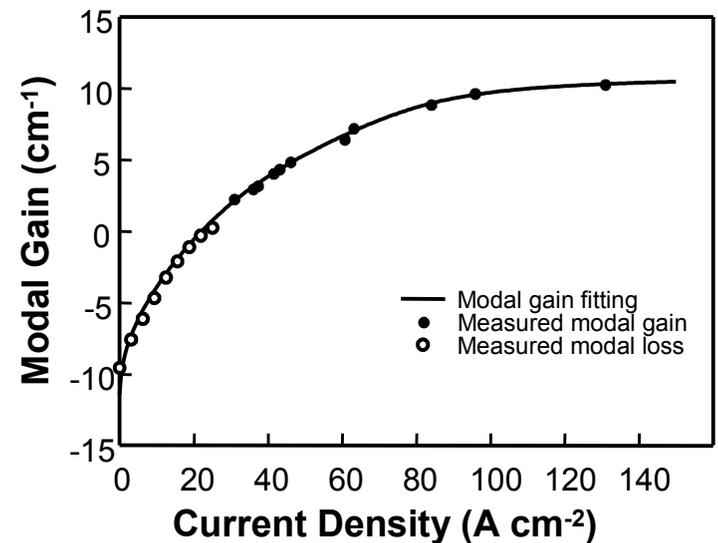
16 ps, 7.4 GHz mode-locked pulses obtained at 1.3  $\mu\text{m}$



Multi-level rate equation model for DWELL lasers



Extensive experimental data helps define large number of parameters



**K. Malloy**

$\tau_c$	$\tau_e$	$\tau_w$	$\tau_{sp0}$	$\tau_{c0}$	$\tau_{e0}$	$(\Gamma g)_{in}$
0.008	2.227	4.279	0.6	0.246	1.385	11.4135



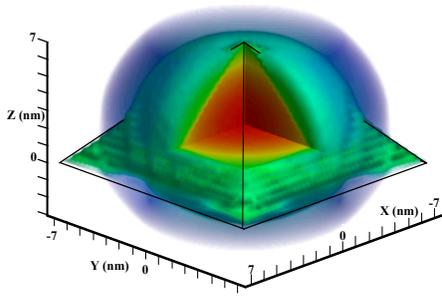
# TAILORING THE PHONON BOTTLENECK

The dot size and shape determines the separation of states  
- and therefore if resonant phonon de-excitation occurs

- Extremely difficult to establish long-lifetime excited states in a solid
- Dot engineering may permit this
- Pathway to efficient detectors and quantum computing devices

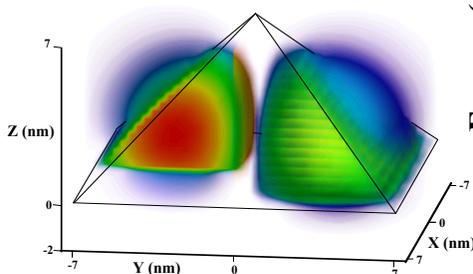
**K. Malloy**

Ground State

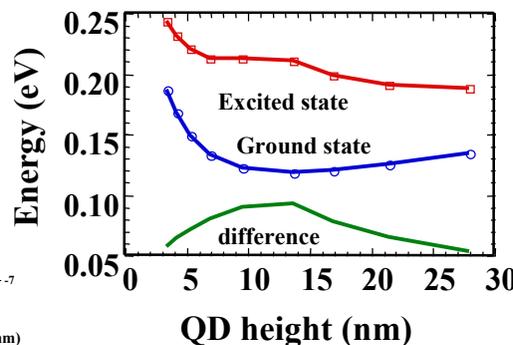


$E_1=184$  meV

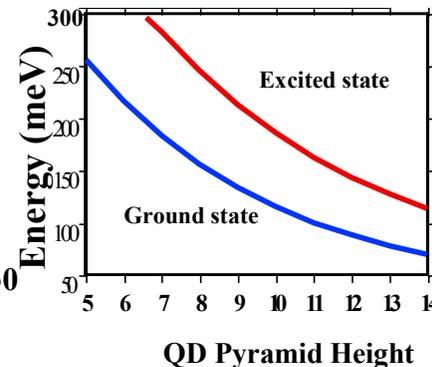
Excited State



$E_2=284$  meV



Constant-Volume  
Quantum Dots

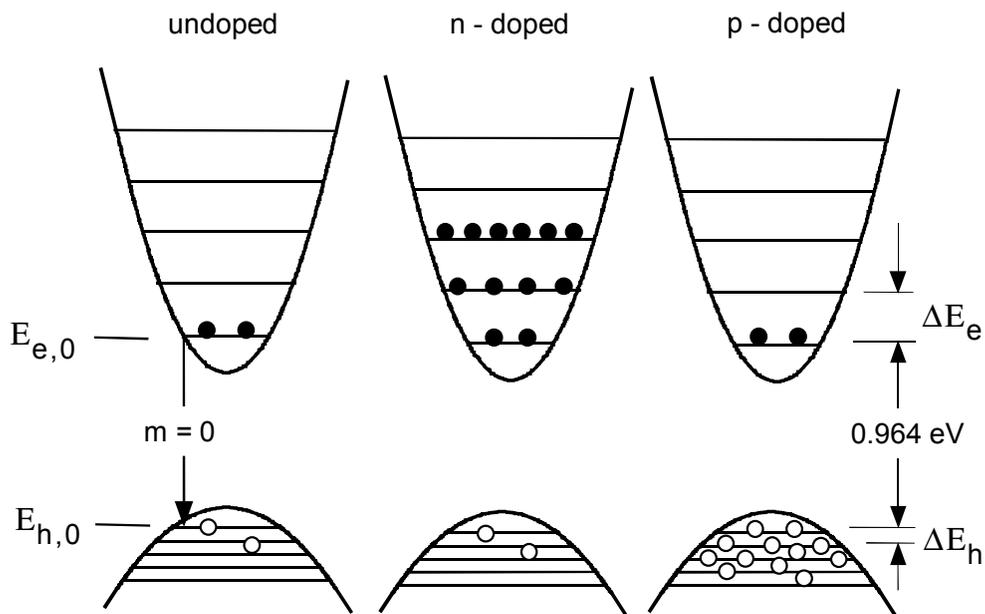


Constant-Base  
Quantum Dots

$m^*=0.07 m$ ,  $\Delta E=300$  meV 14x14x7 nm pyramids

Height a better growth parameter to control  
than base of quantum dot

# INFLUENCE OF DOPING ON QD LASER MODULATION RESPONSE: QUASI-EQUILIBRIUM MODEL

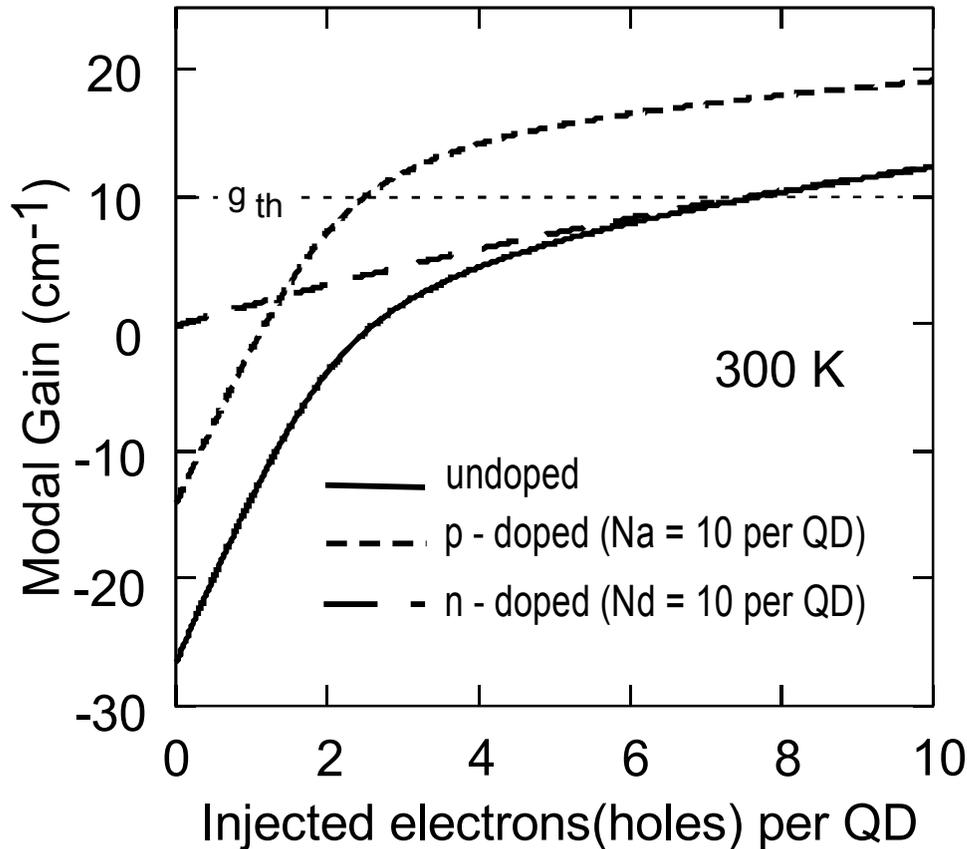


A quasi-equilibrium model of QD lasers shows that their characteristics can be significantly improved through modulation doping to build excess hole carriers into the active region. The improvement is possible due to the close energy spacings of the discrete hole levels.

**D. Deppe**



# CALCULATED MODAL GAIN VS. INJECTED ELECTRONS (HOLES) PER QD

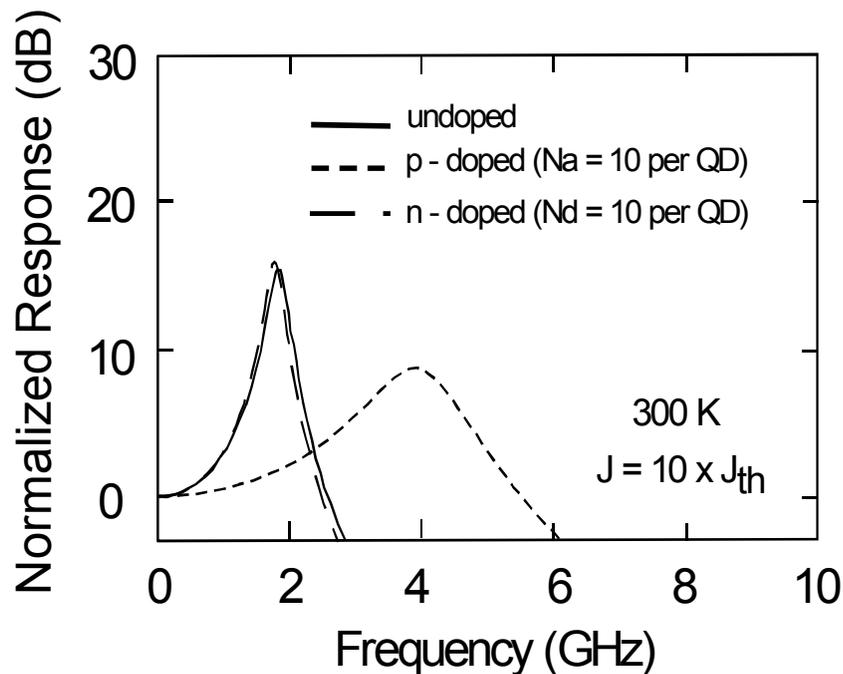
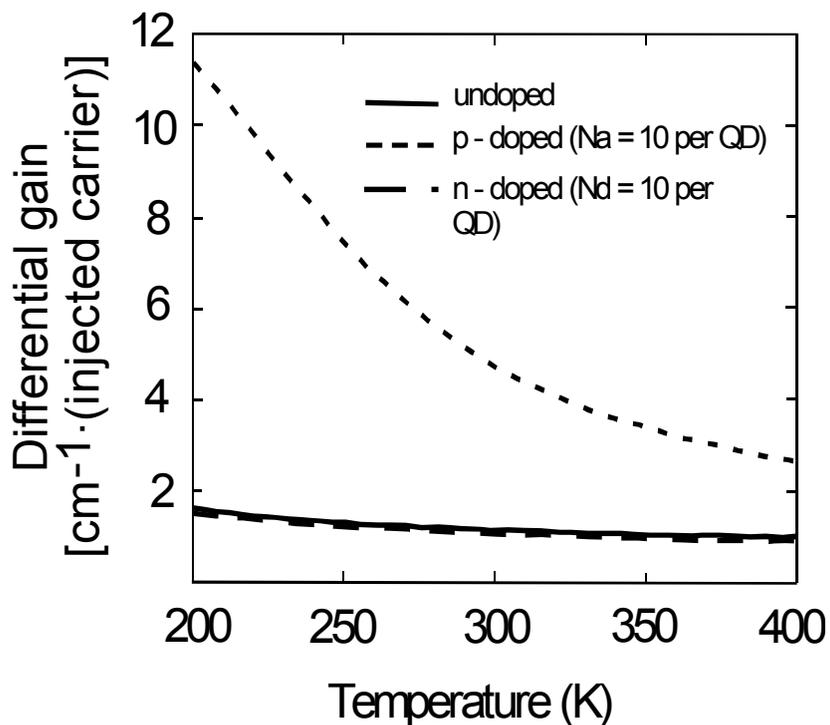


A quasi-equilibrium model shows that p-type modulation doping can significantly increase the optical gain as compared to an undoped or n-type active region. The increase due to the built-in holes is caused by the thermal distribution of carriers and the close energy spacing of the discrete hole levels.

**D. Deppe**



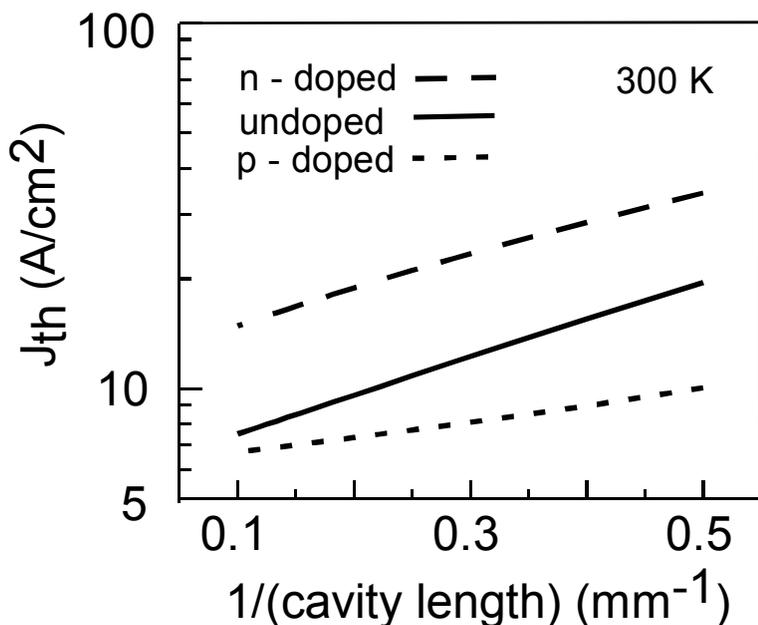
# CALCULATED DIFFERENTIAL GAIN AND IMPACT ON MODULATION RESPONSE



D. Deppe



# CALCULATED THRESHOLD CURRENT DENSITY VS. CAVITY LENGTH FOR DIFFERENT DOPINGS



Calculations show that p-type modulation doping should give a lower threshold current density and smaller dependence of threshold on cavity length than n-type or undoped active regions.

**D. Deppe**



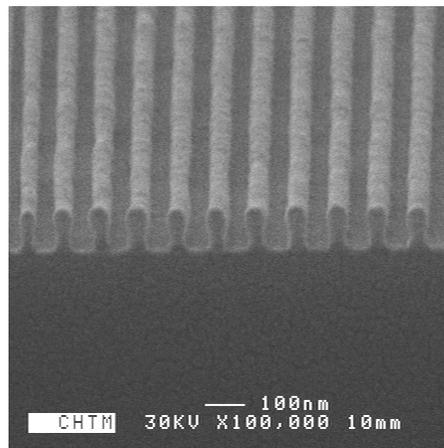
# FUNDAMENTAL LIMITS TO OPTICAL LITHOGRAPHY

- Limit is on the pitch, NOT on the CD.
- For  $NA \rightarrow 1$ , limiting pitch is  $\lambda/2$ . Set by highest spatial frequency beat between optical waves.
- Immersion reduces limiting pitch to  $\lambda/2n$ . ( $n \sim 1.5$ ).
- *Nonlinearities in exposure and pattern transfer increase spatial frequencies on wafer.*
- *Can use this to interpolate to get additional density, i. e. to beat the limiting pitch.*
- ***Conclusion: THERE IS NO FUNDAMENTAL LIMIT TO LITHOGRAPHY, THERE ARE ONLY PROCESS, IMPLEMENTATION AND COST LIMITS.***



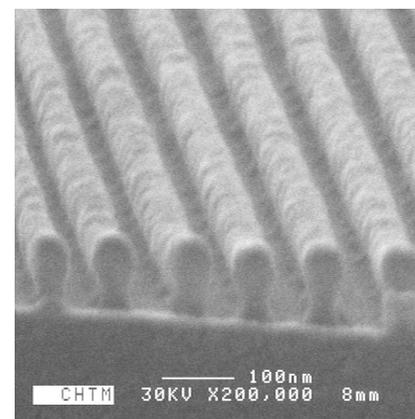
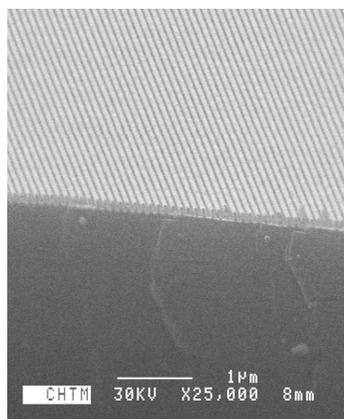
# FUNDAMENTAL LIMITS OF OPTICS EXTEND WELL BELOW $\lambda$

- Optical resolution, linear-systems limits of are on period:
- $[\sim \lambda/2 \sim 200 \text{ nm}/(2) \sim 100 \text{ nm}]$
- Immersion improves result by refractive index:
- $[\sim \lambda/2n \sim 200\text{nm}/(2 \times 1.5) \sim 65\text{nm}]$



CD = 40 nm;  
Pitch = 108 nm

$\lambda = 213 \text{ nm}; \theta \sim 80^\circ$   
(NA ~ 0.986)



CD = 40 nm; Pitch = 108 nm; DI H<sub>2</sub>O  
 $\lambda = 213 \text{ nm}, n = 1.5, \theta = 41^\circ$  (NA = 0.66)

S. R. J. Brueck



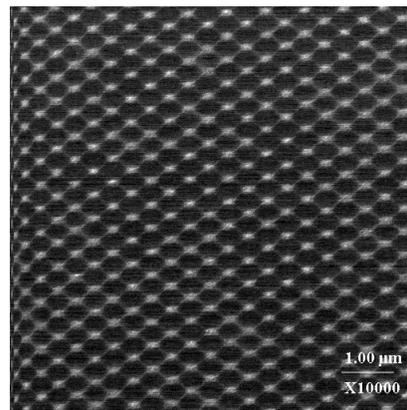
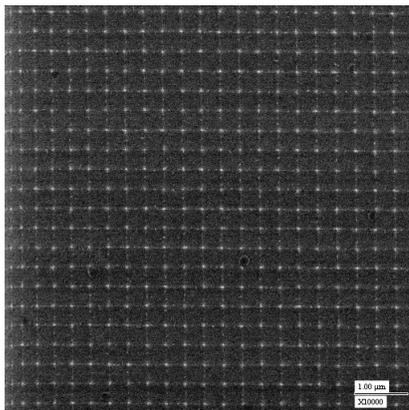
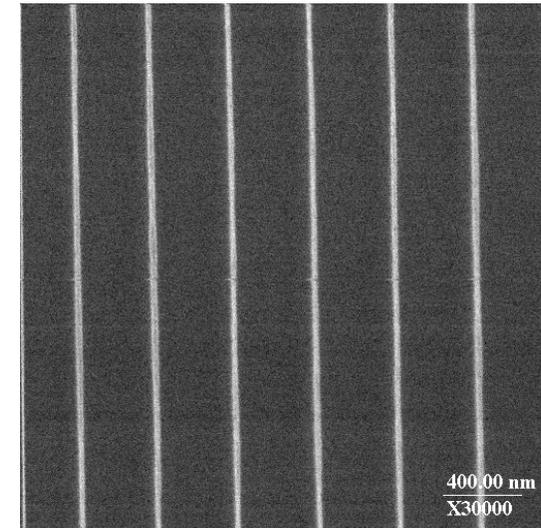
# USE NONLINEAR PROCESSES TO REDUCE LINEWIDTHS WELL BELOW PITCH/2

- Use process nonlinearities to extend to smaller CDs (photoresist expose and develop, etch, sacrificial layers).
- Produces harmonics of fundamental period of optical exposure.
- Accepted practice in industry at limits of resolution - microprocessors (sparse) have smaller features than DRAM (dense).

CD = 30 nm, Pitch = 360 nm

$\lambda = 364$  nm

Oxygen plasma thinning of  
developed photoresist lines.



Si dots on SiO<sub>2</sub> by RIE  
CD ~ 20 nm; Pitch = 360 nm,  
 $\lambda = 364$  nm;  $\theta = 30^\circ$ .



## HOW LOW CAN OPTICS GO?

- For Dense (equal line:space patterns).

	CD	Pitch
■ Frequency space limit is $\lambda/4$	50 nm	100 nm
■ Immersion provides another factor of $\sim 1.5$	33 nm	66 nm
■ Spatial period division provides another factor of 2	17 nm	34 nm
- No fundamental limit on linewidth.
- Optical lithography offers:
  - Scalability to large numbers of nanostructures (34 nm pitch corresponds to density of  $\sim 10^{11}$  cm<sup>2</sup> comparable to self-assembled quantum dot densities).
  - Proven manufacturing capability.
  - Inexpensive platform for nanostructure research.
  - Proven overlay capabilities for multiple levels.



# APPLICATIONS OF INTERFEROMETRIC LITHOGRAPHY

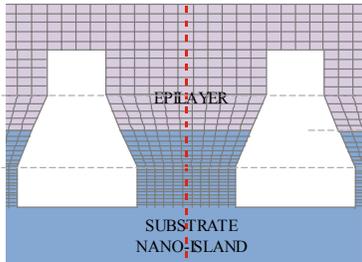
- DFB/DBR lasers (first-order pitch  $\sim \lambda/2n \sim 200$  nm)
- 2D Photonic crystals
  - New laser structures
  - Emission control/enhancement for LEDs
- Nanoscale epitaxial growth
  - Heteroepitaxial growth with large lattice mismatch (GaAs/Si and GaN/Si)
  - Position and size control of quantum dots (InAs/GaAs)
- Large-area artifacts for precise positioning (2D gratings over 12" wafers for transverse interferometers).
- Inexpensive, scalable, manufacturable route to nanoscale ( $< 20$  nm).



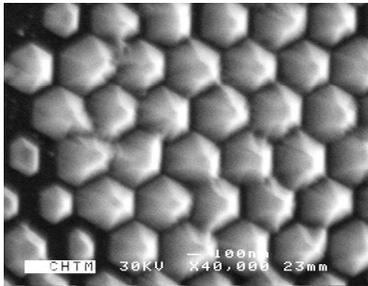
# NANOSCALE GROWTH OFFERS NEW POSSIBILITIES

S. R. J. Brueck /  
L. R. Dawson/ S. D. Hersee

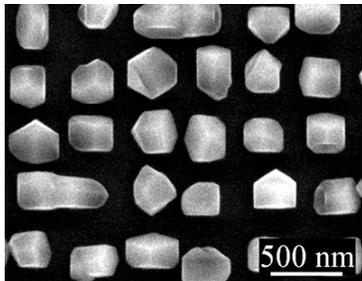
## Nanoheteroepitaxy for Large Lattice Mismatches



Nanoscale  
seeds offer  
potential for  
strain relief.

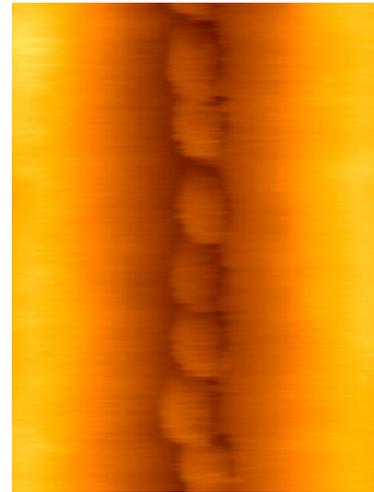


GaN on Si  
(22% lattice  
mismatch!)

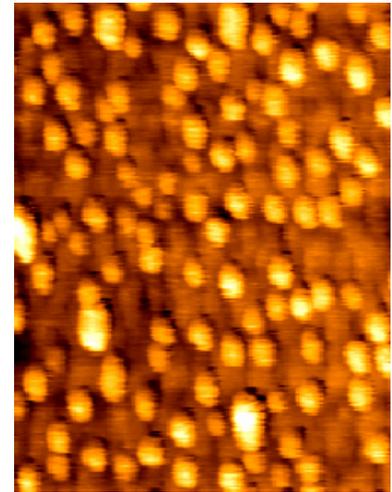


GaAs on Si  
(4.2% lattice  
mismatch)

## Nanoscale Growth for Manufactured Quantum Dots



Combining  
lithography  
and self  
assembly gives  
1D lines of  
quantum dots



Self assembly  
on planar  
surface gives  
random array  
of quantum  
dots

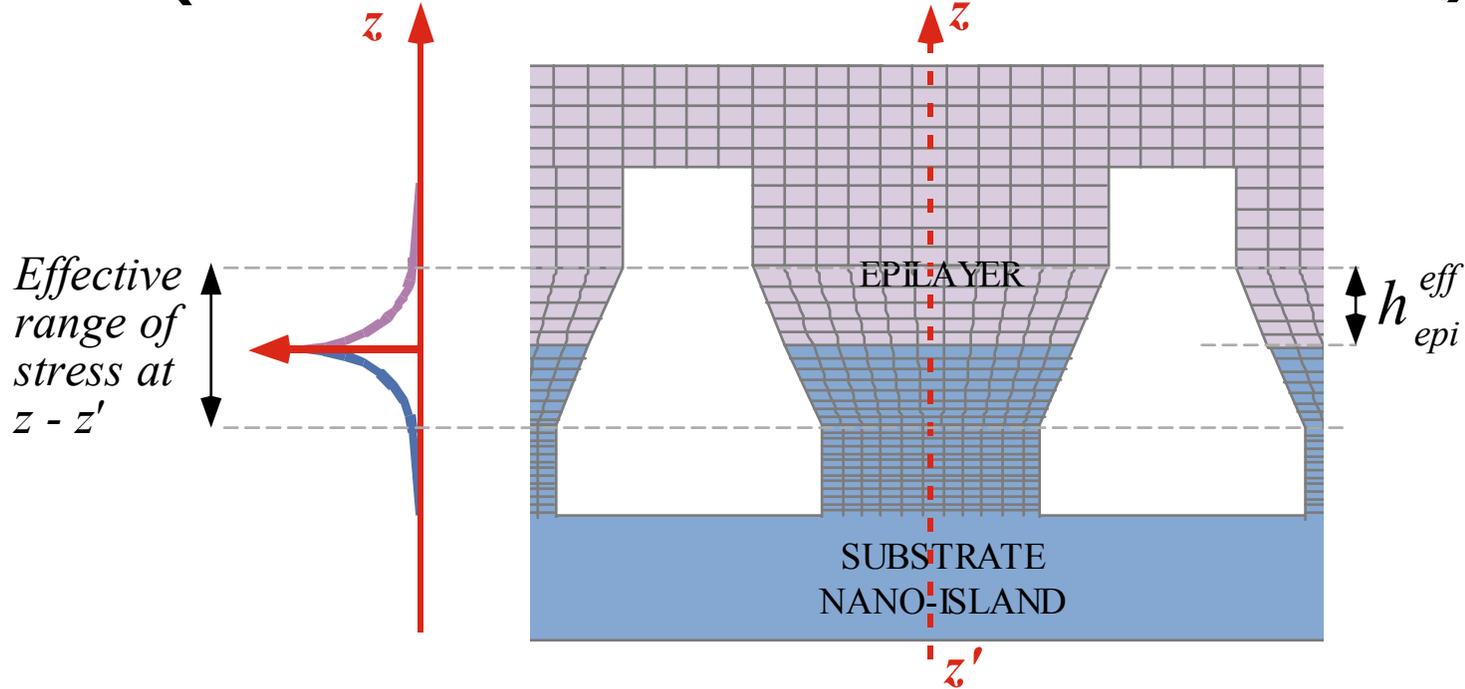


# **NANO HETEROEPITAXY IS A NEW APPROACH TO LATTICE MISMATCHED MATERIALS GROWTH**

- NHE is a new heteroepitaxial approach
  - Growth initiated on nanoscale seeds
  - 3-D stress relief mechanisms utilized to reduce strain energy and inhibit formation of defects
- How is NHE different from other heteroepitaxial approaches?
  - Differentiating feature is growth on dense periodic array of nanoscale structures
  - **Nanofabrication is enabling technology for NHE**

**S. D. Hersee  
S. R. J. Brueck**

# NHE (3D STRESS RELIEF AND COMPLIANCE)



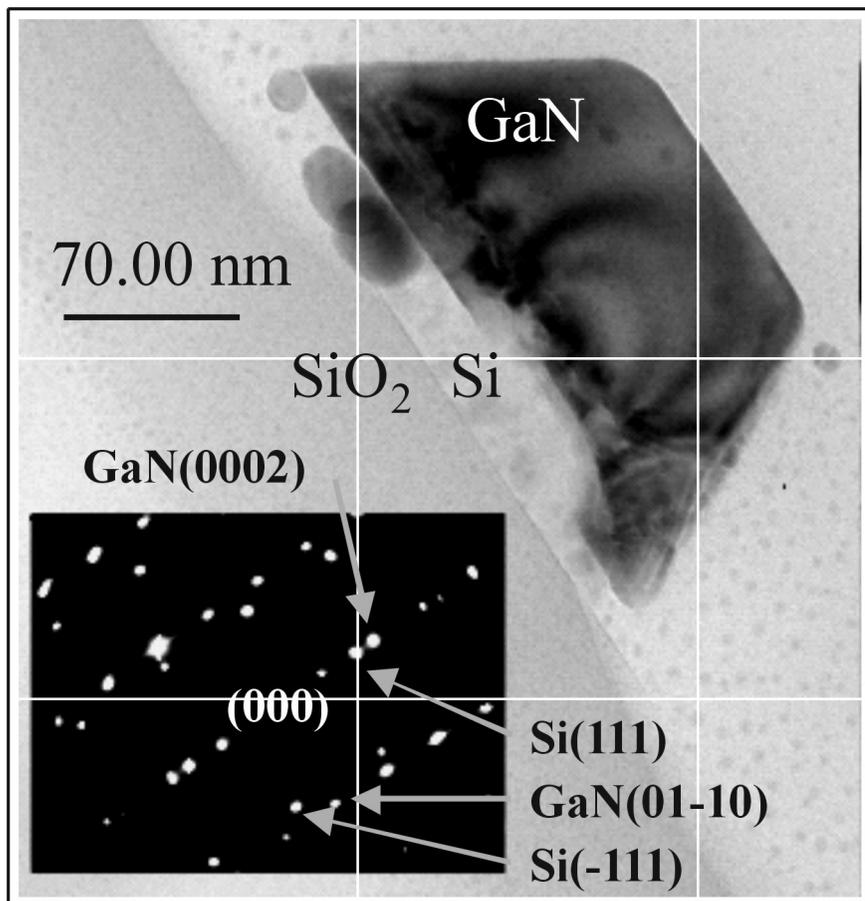
NHE theory [1] combines 3D stress relief and substrate compliance. Stress and strain decay exponentially on both sides of heterointerface.

Strain energy saturates  $h_{epi} > h_{epi}^{eff}$

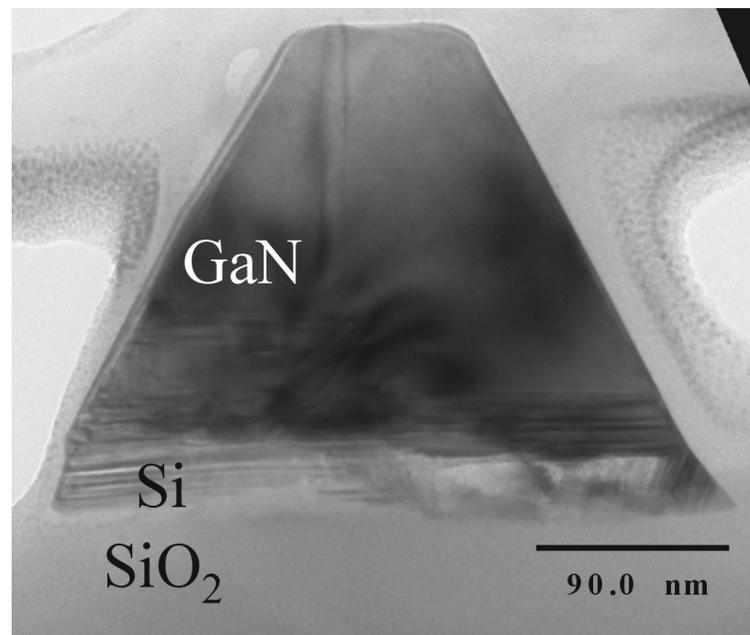
**S. D. Hersee**  
**S. R. J. Brueck**

[1] "Nanoheteroepitaxy: A New Approach to the Heteroepitaxy of Mismatched Semiconductor Materials", D. Zubia, S.D. Hersee, J. Appl. Phys., **85** (1999) 6492 - 6496

# GaN ON PATTERNED SOI: NANOHETEROEPITAXY



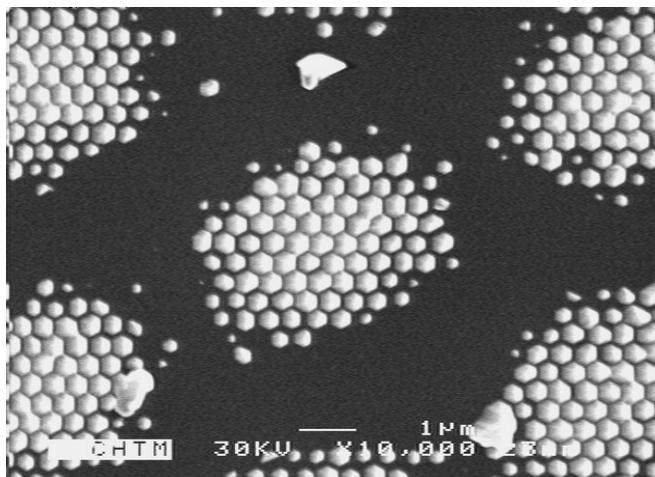
Strain field in epilayer indicates decaying strain  
 Defects in silicon and GaN indicate strain partitioning  
 Alignment of GaN[0002] and Si[111] SOI acting as epitaxial template.



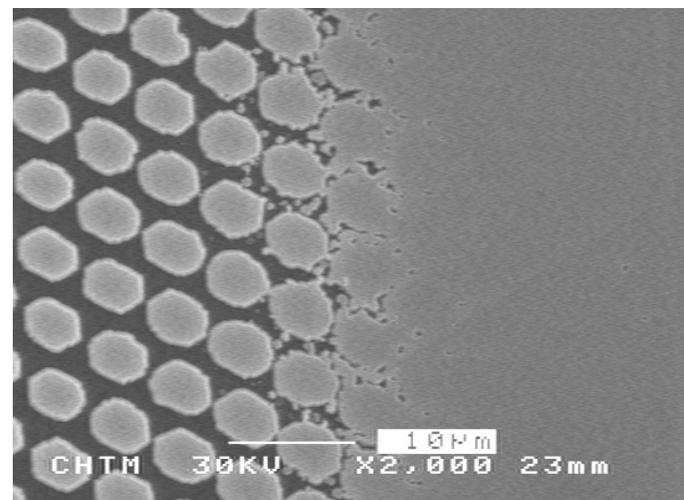
S. D. Hersee  
S. R. J. Brueck

# NANOHETEROEPITAXY (NHE)

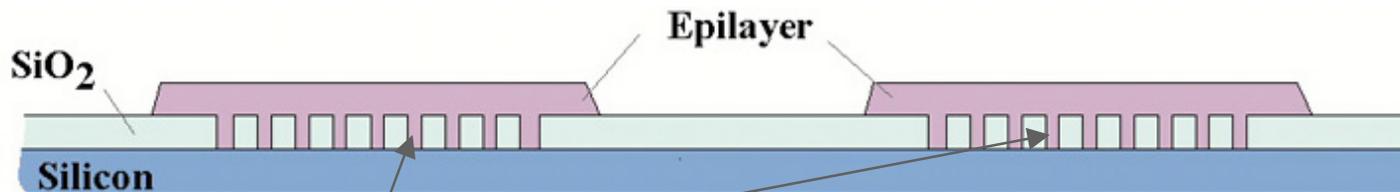
**Concept:** Mismatched materials technologies can be combined on nanoscale patterned substrates



0.1 μm GaN on Si (22% mismatch)



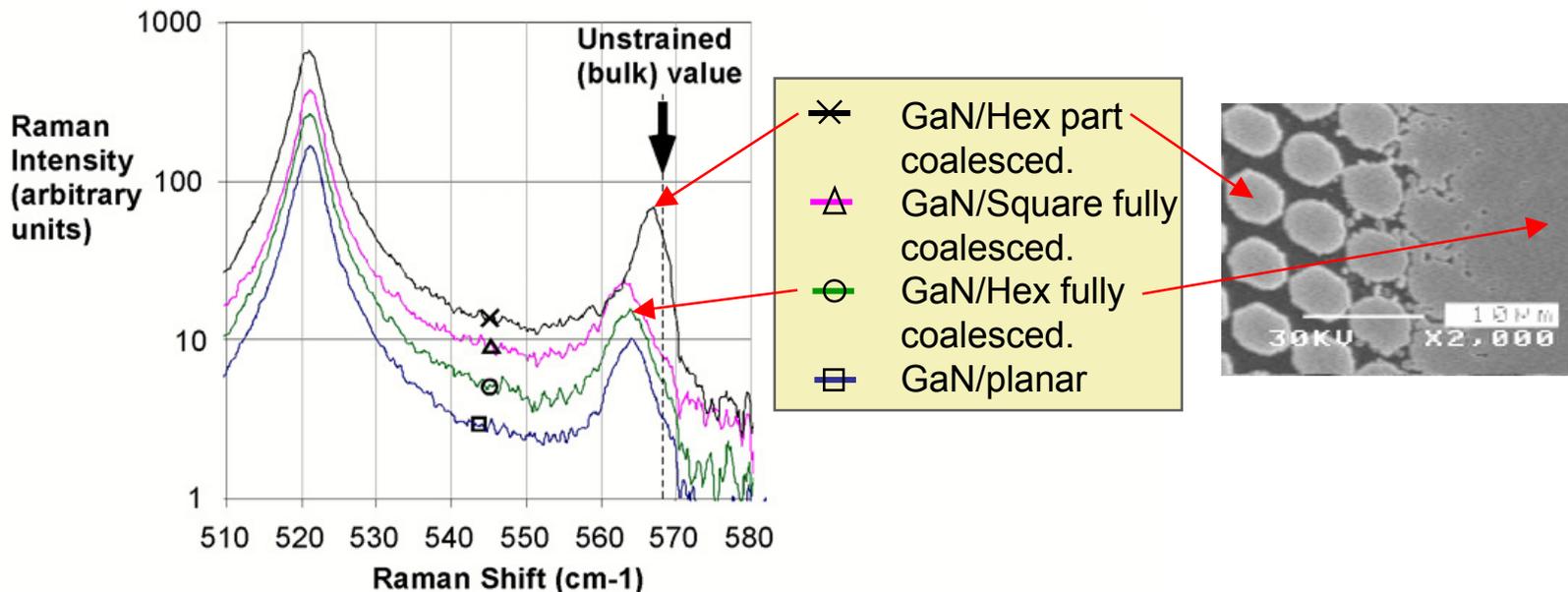
2.0 μm GaN on Si (22% mismatch)



nanoscale patterning allows large strain relief through 3D deformation of nanoscale nuclei. 3D deformation is not available to larger nuclei.

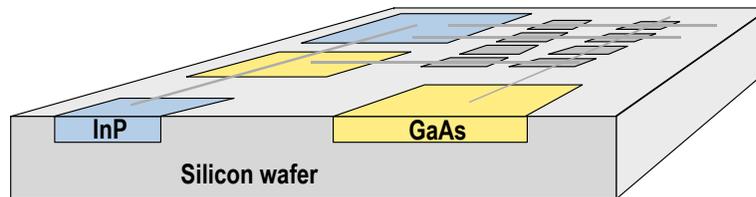
S. D. Hersee  
S. R. J. Brueck

# STRAIN IN NHE GaN ON Si



Tensile strain in fully coalesced regions -0.51 GPa (cracking)  
Tensile strain in partially coalesced regions -0.09 GPa (no cracking)  
(Raman measurements confirmed by shift of room temperature PL peak)

Application is integration of III-V and Si technologies - adding extra performance and functionality to silicon.



S. D. Hersee  
S. R. J. Brueck



# NANO HETEROEPITAXY SUMMARY

- NHE is a new paradigm for heteroepitaxy that predicts reduced strain energy, due to 3D relaxation and strain partitioning.
- Coherent epitaxial islands of arbitrary thickness can be grown on materials systems with lattice mismatch up to 4.5% provided the island diameter is sufficiently small ( $\sim 20 - 50$  nm).
- Experimental results show a dramatic improvement in the quality of the GaN grown on nanostructured (111) SOI compared to planar growth.
- PL data showed a 25x brighter band-edge emission from GaN grown on the nanostructured sample compared to planar samples.
- NHE should be widely applicable to many materials systems.
- Future work will concentrate on achieving macro-scale, defect-free coalescence.