



High Capacity
Optoelectronic
Interconnects

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ENGINEERING NANOSTRUCTURES – ENABLING TECHNOLOGIES

Interferometric lithography for nanostructure fabrication.

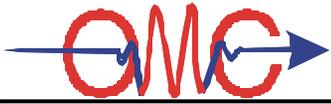
-  Limits of optical lithography are deep nano-scale.
-  Applications to integration and devices.

S. R. J. Brueck

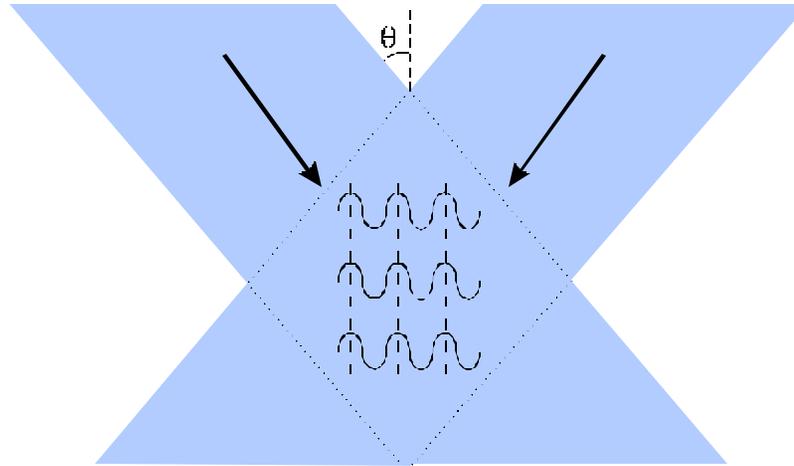
Nanoheteroepitaxial growth for integration with Si substrates.

-  GaN and GaAs on Si.
-  Strain relief from nanoscale relaxation.
-  Improved PL from GaN on Si.

S. D. Hersee



INTERFEROMETRIC LITHOGRAPHY



- Large areas with sub- λ periodicity ($\lambda/2\sin\theta$) at practical fluences.
- Fundamental limit is on period, not on linewidth. Nonlinearities in resist processing provide higher harmonics and narrower features with vertical sidewalls.
- ∇ depth-of-field on scale of Si processing.
- Simple, low NA optics.

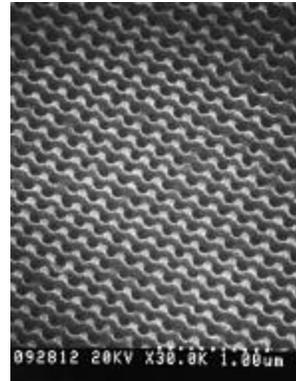


FUNDAMENTAL LIMITS OF OPTICS EXTEND WELL BELOW I

 **Optical resolution, linear-systems limits of are on period**

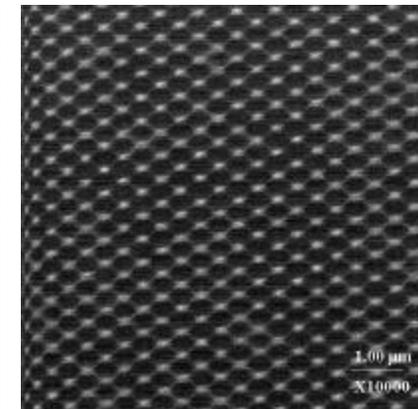
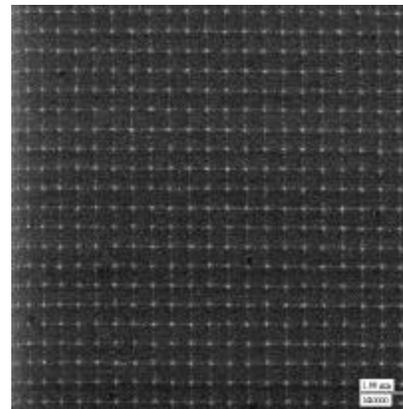
$$[\sim \lambda/2n \sim 200 \text{ nm}/(2 \times 1.5) \sim 70 \text{ nm}]$$

not on linewidth or CD.



**CD = 90 nm;
Pitch = 180 nm**

? = 364 nm; ? ~ 75°

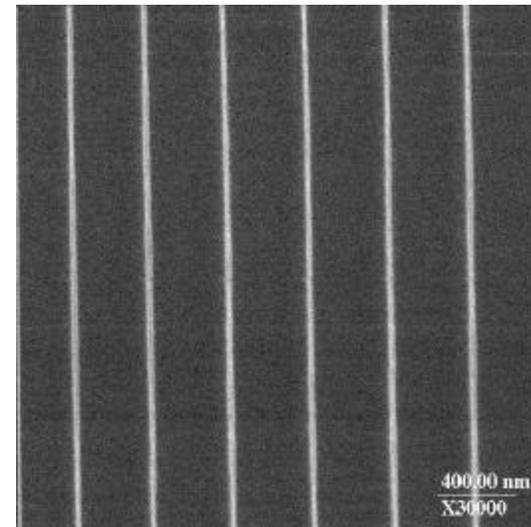


**CD ~ 20 nm; Pitch = 360 nm,
? = 364 nm; ? = 30°.**



USE NONLINEAR PROCESSES TO REDUCE LINEWIDTHS

- ✍ Use process nonlinearities to extend to smaller CDs (photoresist expose and develop, etch, sacrificial layers, ...).
- ✍ Produces harmonics of fundamental period of optical exposure.
- ✍ Accepted practice in industry at limits of resolution - microprocessors (sparse) have smaller features than DRAM (dense).



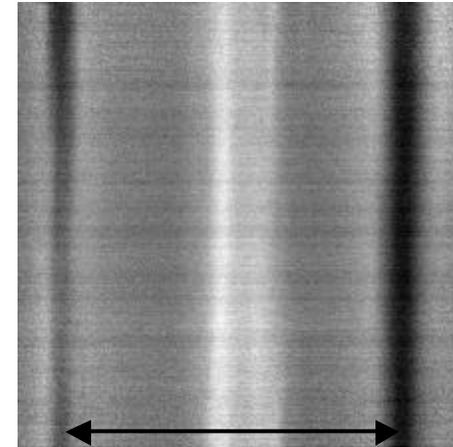
CD = 30 nm, Pitch = 360 nm
? = 364 nm

Oxygen plasma thinning of developed photoresist lines.



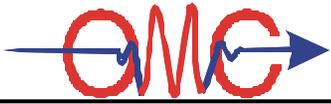
COMBINING NONLINEARITIES CAN INCREASE DENSITY

- ✍ Since limit is on pitch, not CD.
 - ✍ Write first pattern at small CD.
 - ✍ Interpolate second pattern.
 - ✍ Result is a denser pattern from optics.
- ✍ Requires extra processing.
Need to apply nonlinearities separately to individual exposures.
- ✍ Interlevel alignment is a strength of optical lithography.



400 nm

Photoresist line
interpolated between
two existing lines



HOW LOW CAN OPTICS GO?

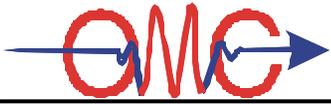
For Dense (equal line:space patterns).

-  Frequency space limit is 1/4 (50 nm)
-  Immersion provides another factor of ~ 1.5 (33 nm)
-  Spatial period division provides another factor of 2 (17 nm)

No fundamental limit on linewidth.

Optical lithography offers:

-  Scalability to large numbers of nanostructures (density of $\sim 10^{11}$ cm²).
-  Proven manufacturing capability.
-  Proven overlay capabilities for multiple levels.
-  Inexpensive platform for nanostructure research.

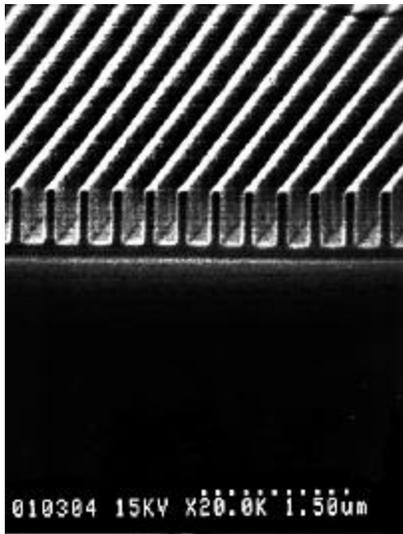


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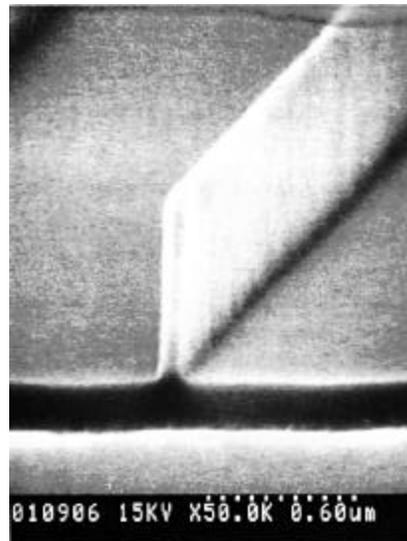
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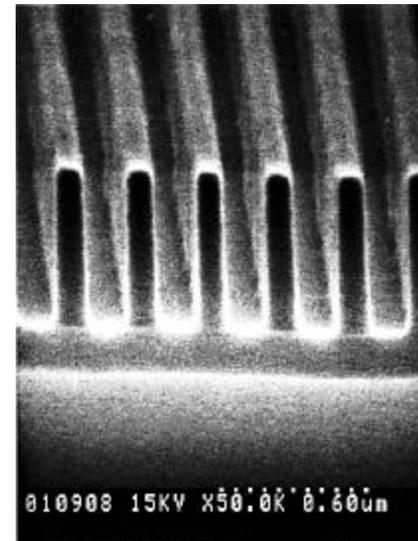
INTERFEROMETRIC LITHOGRAPHY PROVIDES SUB- 150-nm CDs OVER LARGE (cm²) AREAS



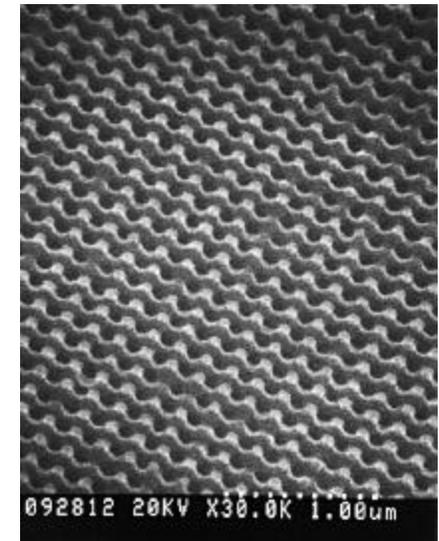
CD = 100 nm
Pitch = 360 nm



CD = 50 nm
Pitch = 2 mm



CD = 150 nm
Pitch = 300 nm

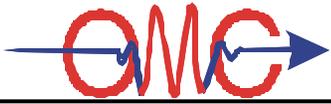


CD = 90 nm
Pitch = 180 nm

**All results at I-line (365 nm) with industry standard
resists.**

**1D results limited by photoresist mechanical properties,
not optics.**

Approved for public release, distribution unlimited

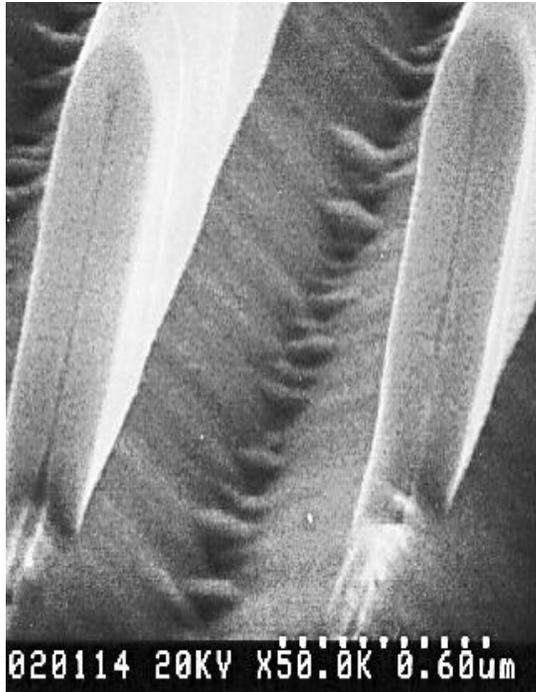


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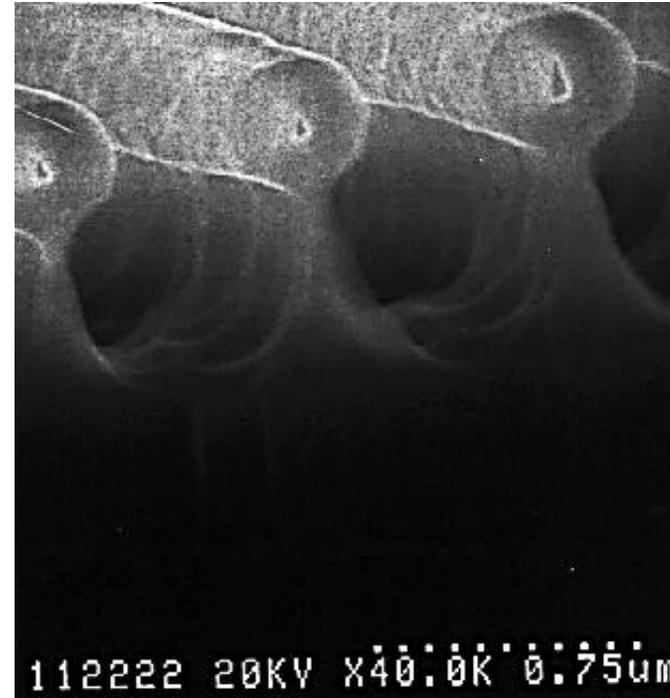
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Si QUANTUM WALLS AND WIRES



**20-nm Walls buried in
oxide**



**30-nm Wires buried in
oxide on SOI**

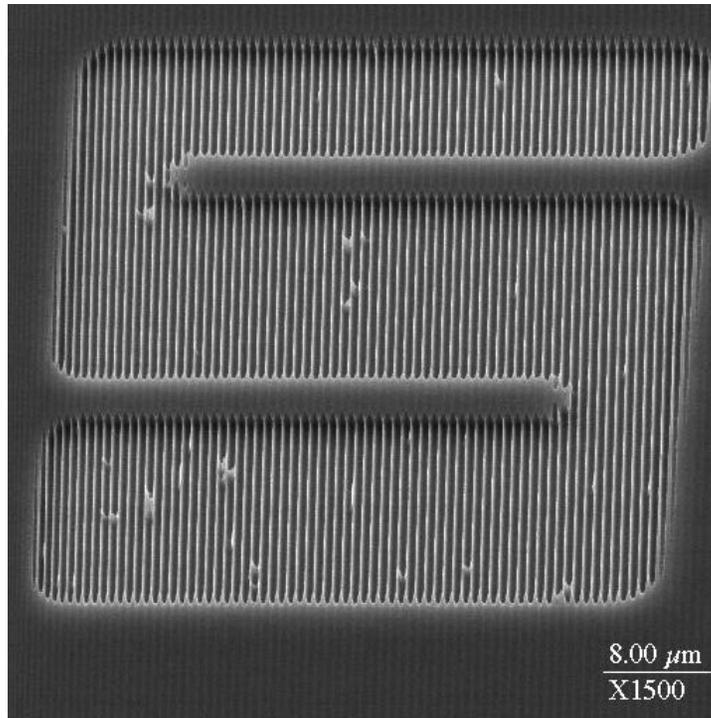


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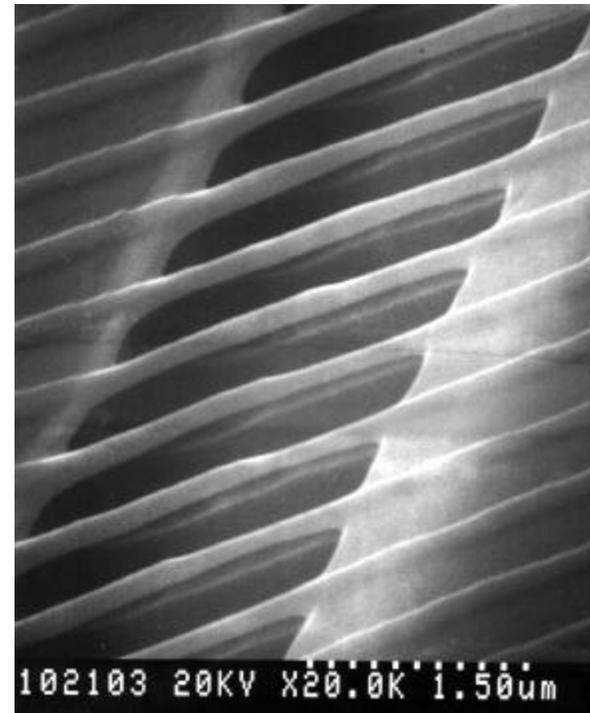
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INTERDIGITATED QUANTUM WIRE DETECTOR



**Microstructure by
conventional
lithography**



**Nanostructure by
interferometric
lithography and
oxidation**

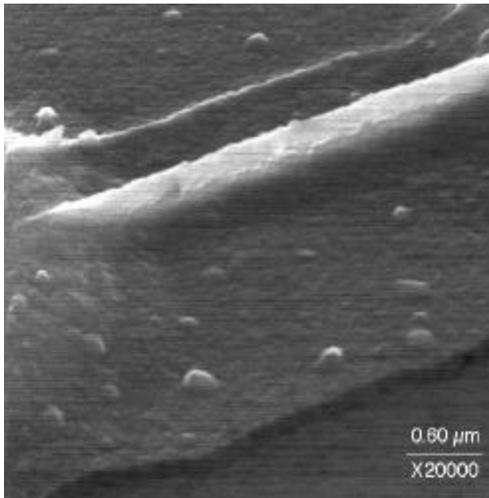
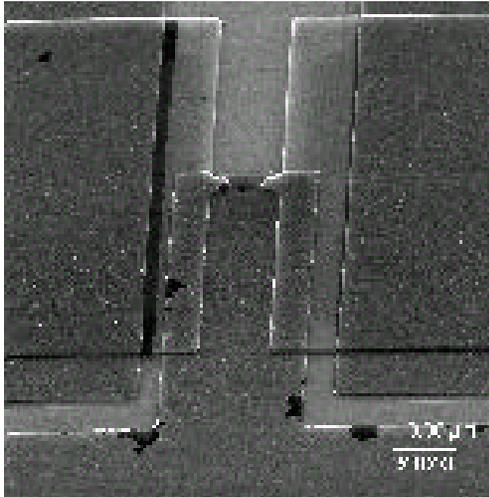


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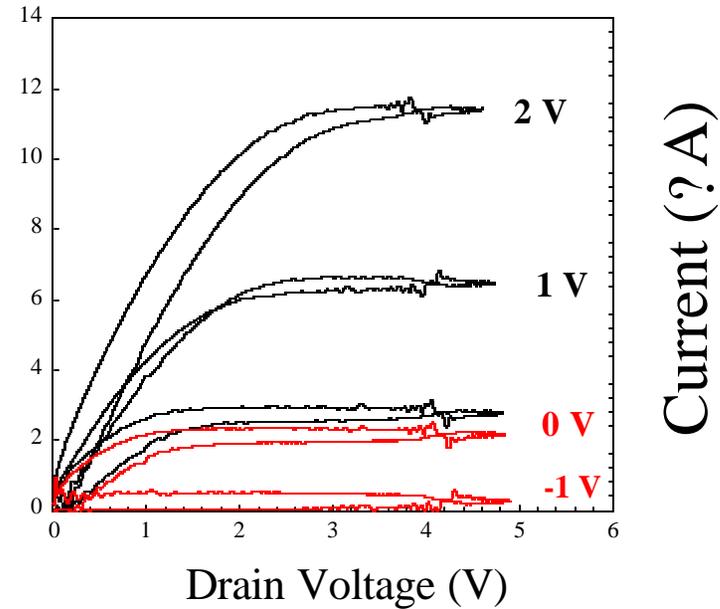
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SINGLE QUANTUM WIRE TRANSISTOR



1 V MOSFET in Depletion Mode Variation With Gate Voltage

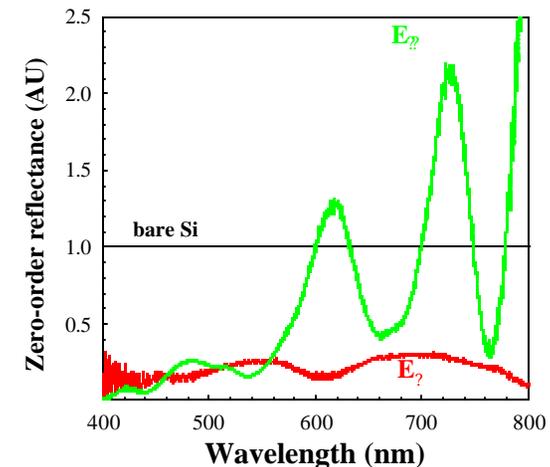
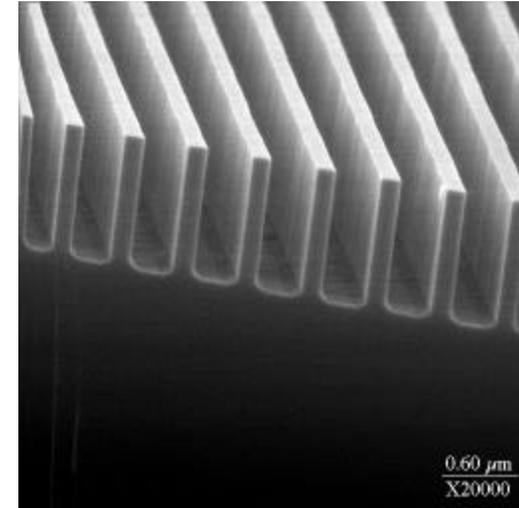


Courtesy of Gratings, Inc.



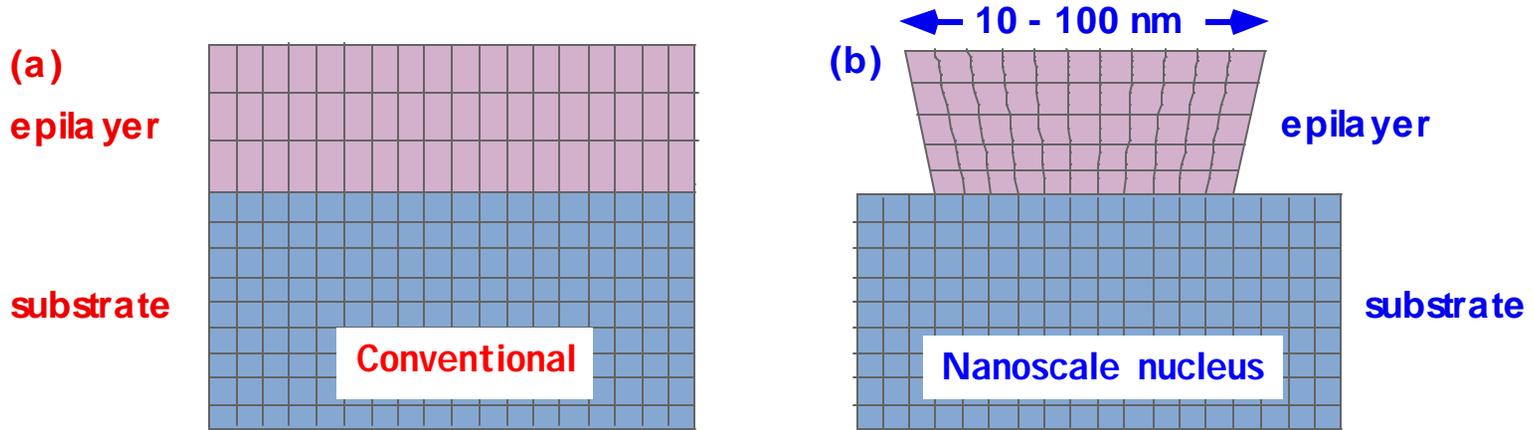
SOME APPLICATIONS OF LARGE-AREA NANOSCALE LITHOGRAPHY

- ▶ Artificial dielectrics (form birefringence, photonic crystals).
- ▶ Physical-optics enhanced photodetectors and emitters.
- ▶ Nano-hetero-epitaxy (growth on a bed of “nanoneedles”).
- ▶ Novel electronic devices (quantum wire transistors, single-electron transistors).
- ▶ Superconducting thin film devices (array of pinning sites controls local conductivity).



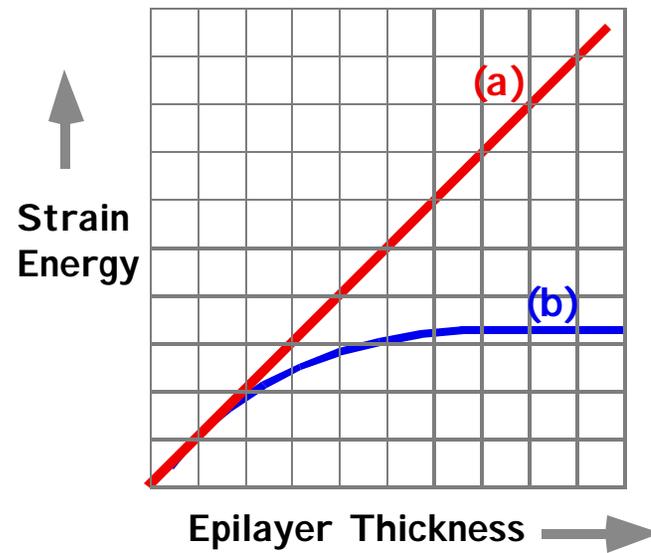


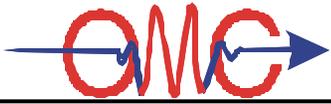
STRESS RELIEF DURING HETEROEPI TAXY



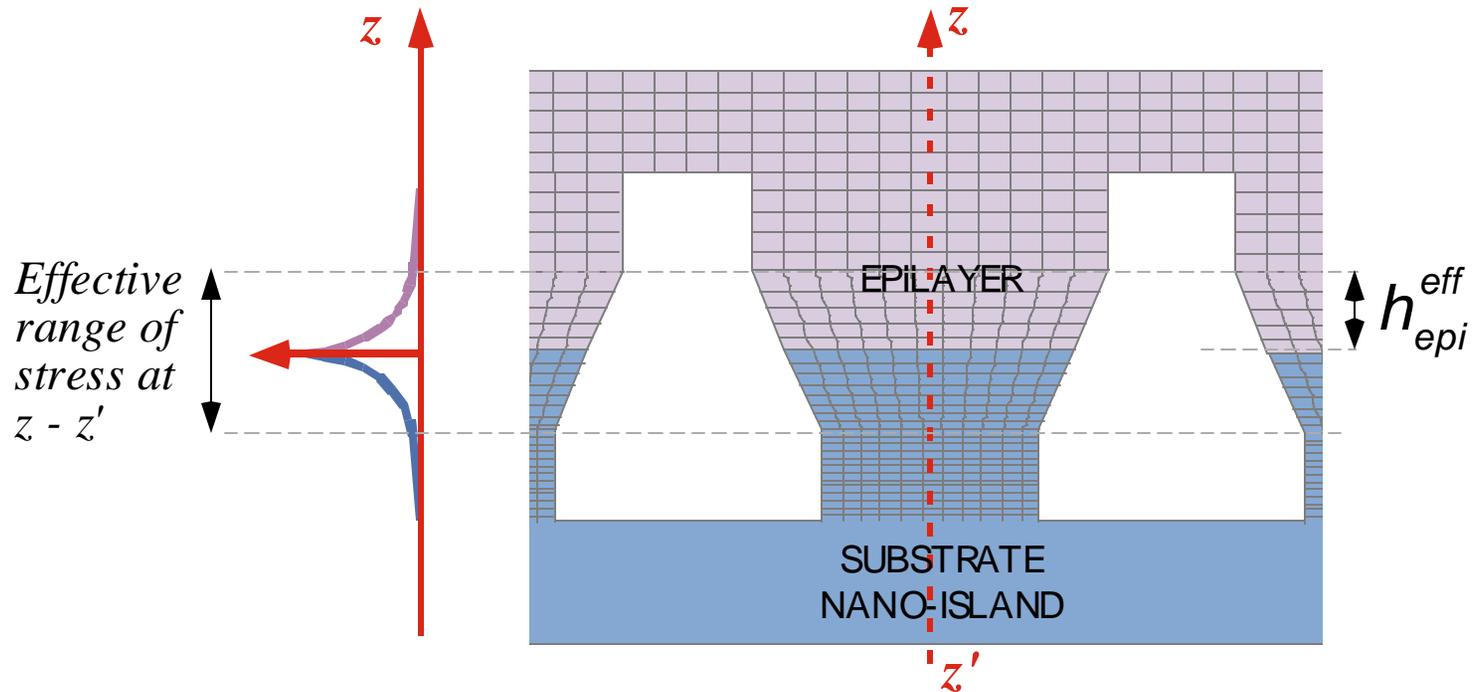
(a) Conventional Heteroepitaxy
Strain at growth interface remains constant and strain energy grows linearly with epilayer thickness. Dislocations eventually created.

(b) Stress relief in Nanosize Nucleus
3-D strain in nanosize nucleus gives exponential stress/strain decay (Luryi and Suhir, 1986). Decay length is proportional to (and of similar magnitude to) island diameter. Strain energy saturates at a maximum value.





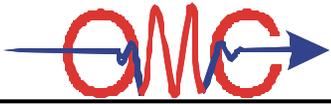
NHE (3D STRESS RELIEF AND COMPLIANCE)



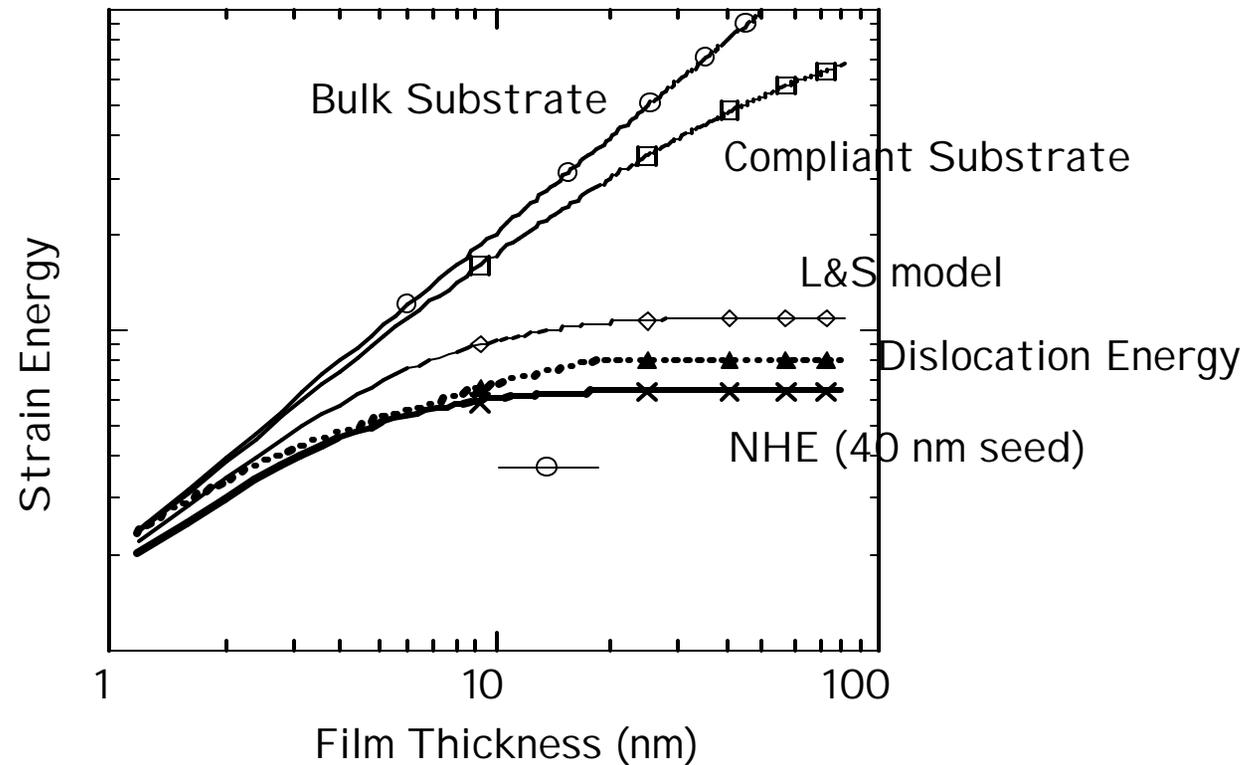
NHE theory [1] combines 3D stress relief and substrate compliance. Stress and strain decay exponentially on both sides of heterointerface.

Strain energy saturates when $h_{epi} > h_{epi}^{eff}$

[1] "Nanoheteroepitaxy: A New Approach to the Heteroepitaxy of Mismatched Semiconductor Materials", D. Zubia, S.D. Hersee, J. Appl. Phys., **85** (1999) 6492 - 6496



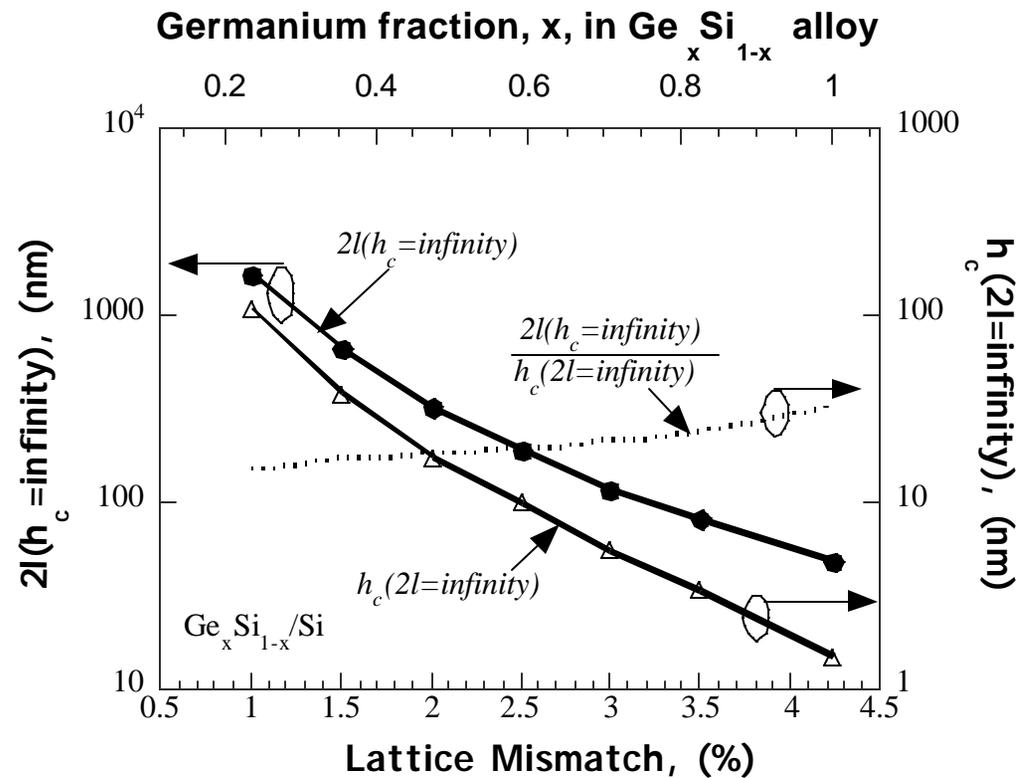
NANOHETEROEPITAXY OF GaAs ON Si

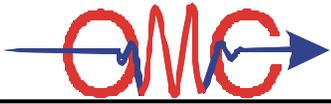


Theoretical comparison of heteroepitaxy approaches for GaAs on Si. (Nano-island diameter = 40 nm)



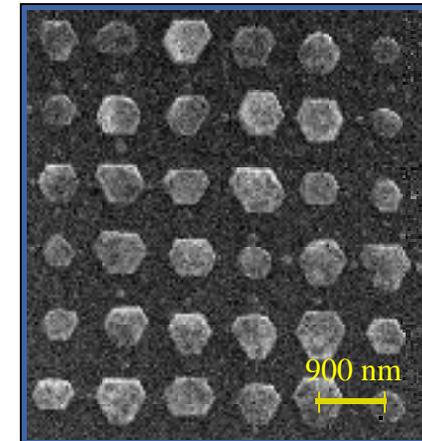
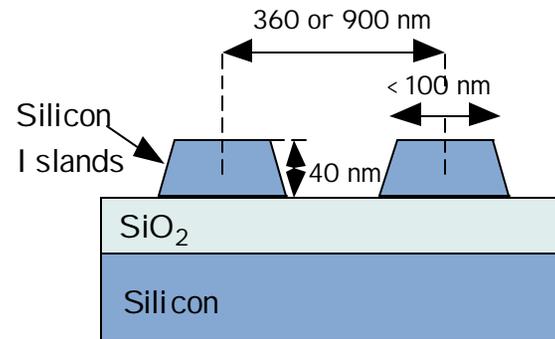
MAXIMUM ISLAND SIZE CLOSELY RELATED TO CRITICAL THICKNESS FOR DEFECT-FREE GROWTH



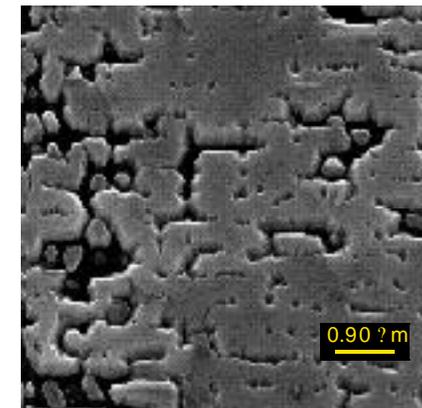
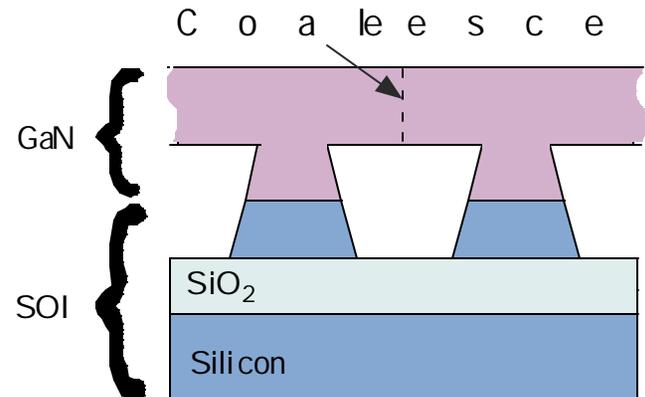


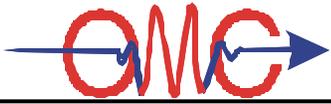
NANOSTRUCTURED SOI SUBSTRATE FOR GaN NHE

I: Interferometric lithography patterns silicon layer on silicon on insulator (SOI) substrate. Creates nanosize growth islands. SiO₂ provides selectivity during OMVPE

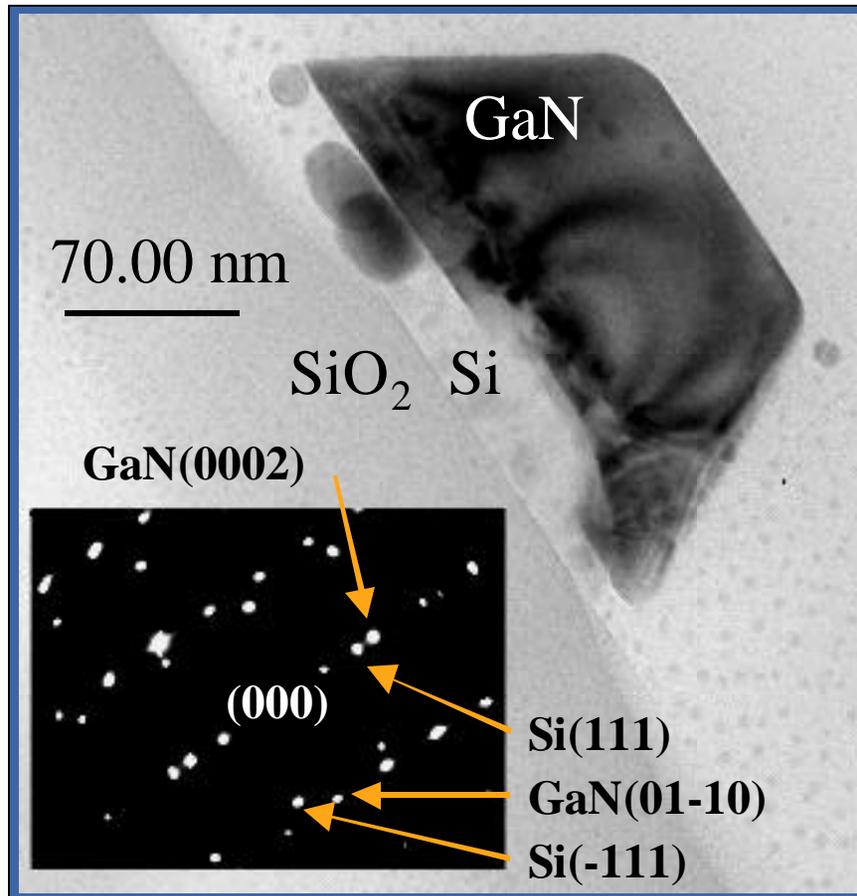


II: OMVPE selective growth is used to grow GaN on nanosize Si islands. Lateral growth is later promoted to allow coalescence of GaN film.





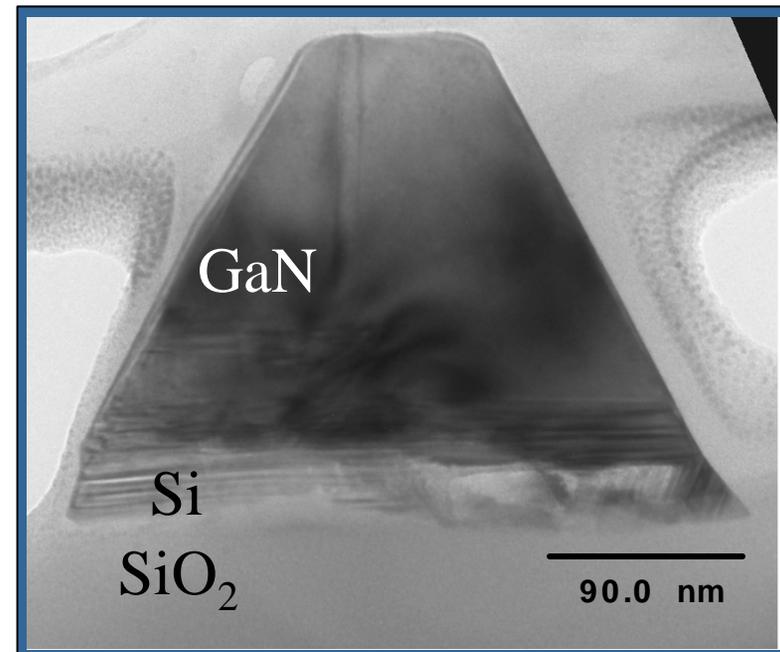
GaN ON PATTERNED SOI: NANOHETEROEPI TAXY



Strain field in epilayer indicates decaying strain

Defects in silicon and GaN indicate strain partitioning

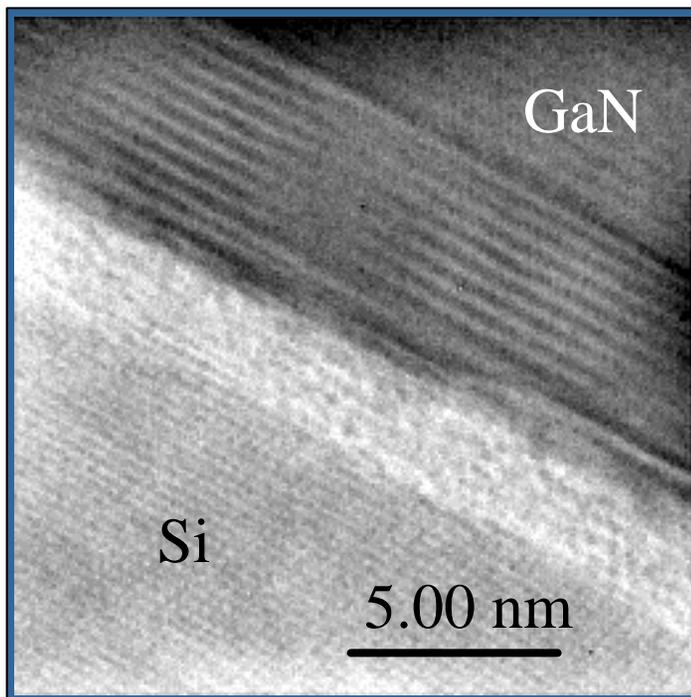
Alignment of GaN[0002] and Si[111] SOI acting as epitaxial template.



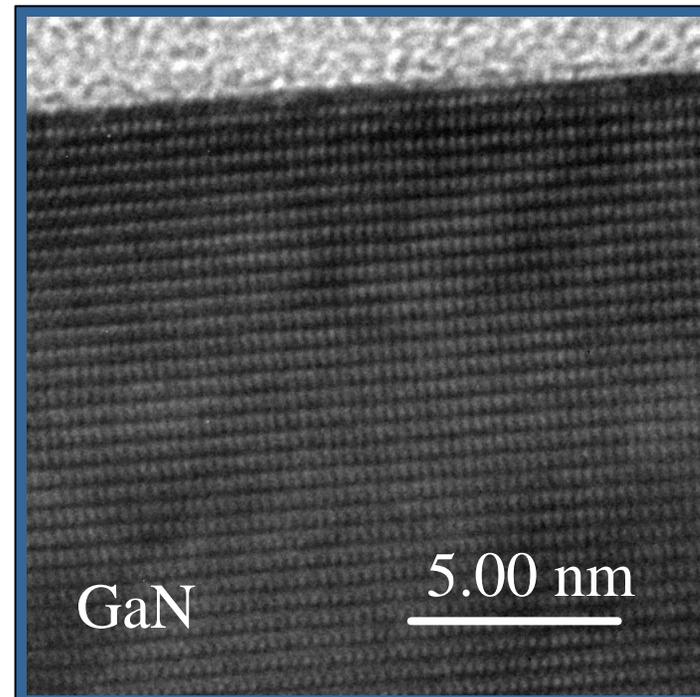


HIGH RESOLUTION XTEM OF NHE GaN ON Si

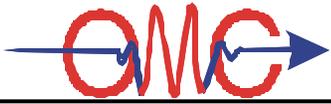
HRTEM reveals that defects are confined to heterointerface region. In GaN defects are mainly stacking faults. Silicon close to the interface is almost amorphous, indicating large amount of strain taken up by silicon.



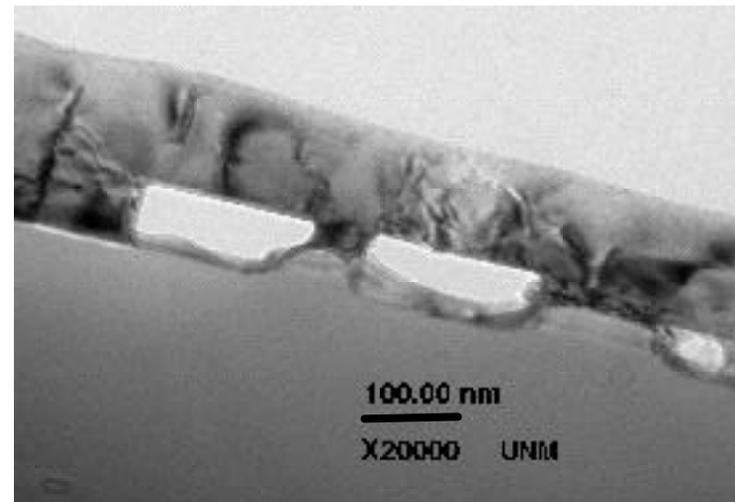
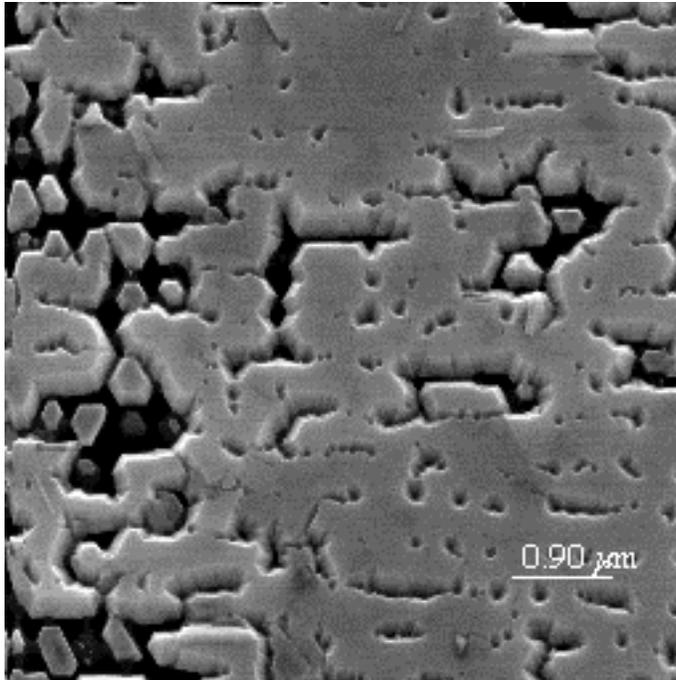
GaN/Si interface



Top of GaN island



COALESCENCE DURING NHE GROWTH OF GaN ON Si

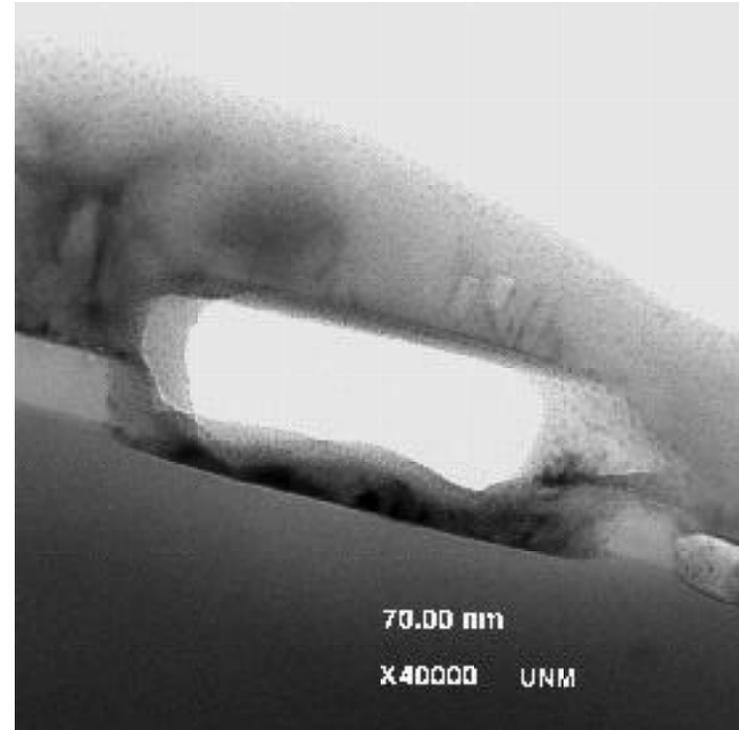
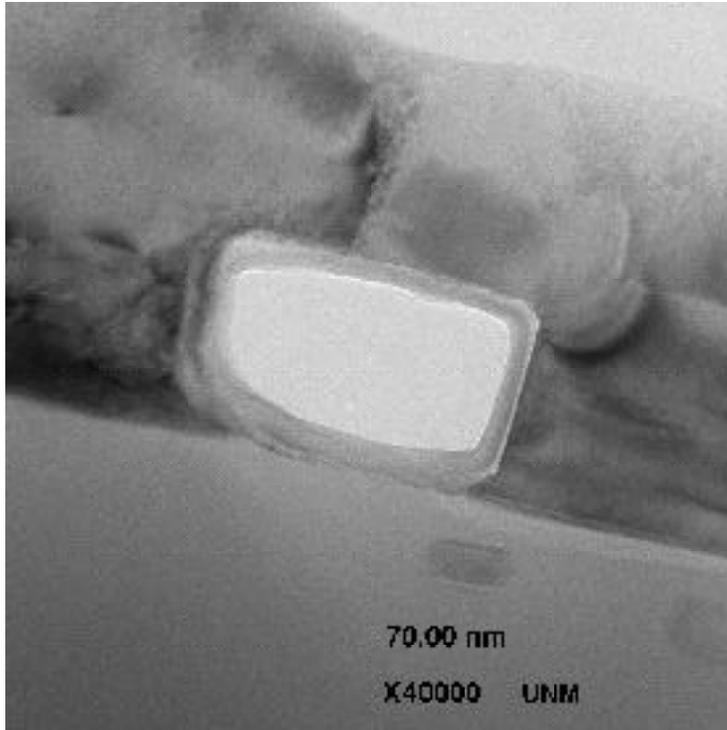


Uniformity of nano-island size and spacing is critical as it controls:

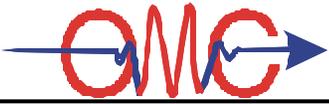
- strain decay length and defect density according to NHE theory
- growth rate at nano-island during selective growth regime
- properties of Si nano- nucleus



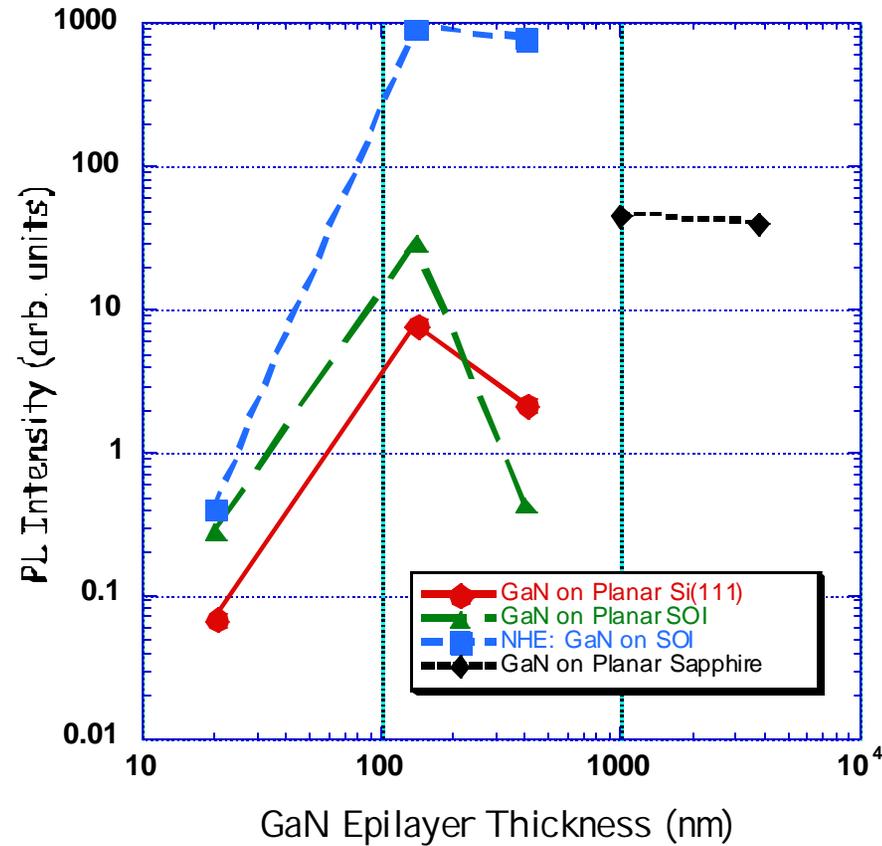
NHE COALESCENCE: GaN ON Si



Preliminary XTEM analysis of coalescence in NHE samples reveals 2 types of behavior. In some samples the coalescence region appears to be defect free.



ROOM TEMPERATURE, GaN PL INTENSITY





CONCLUSIONS

- ▶ **Interferometric lithography for nanostructure fabrication:**
 - Large-area nanoscale capability to ~ 20 nm (density ~ 10^{11} cm⁻²).
 - Use nonlinear processes to decrease CDs and increase density.
 - Mix-and-match with optical lithography for device structures.
- ▶ **Nanoheteroepitaxy for heterogeneous integration:**
 - ▶ 3D strain relief provides new regime for heteroepitaxy.
 - ▶ Promising initial results on GaN on Si and GaAs on Si.
 - ▶ Local free surface changes defect character.