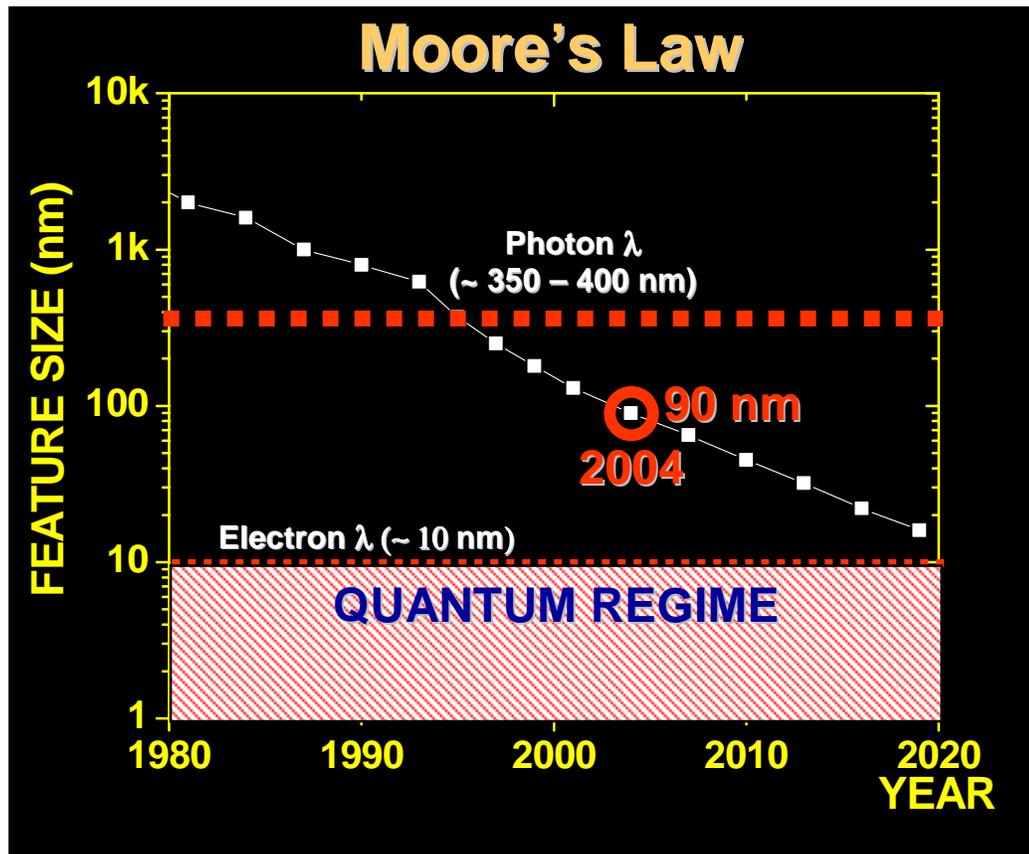


EPIC

Electronic & Photonic Integrated Circuit

An extraordinary opportunity, to create a seamless interface between electronics and photonics in Silicon, is beginning to emerge, and the Microsystems Technology Office of DARPA is about to launch a new program to exploit this opportunity.

The opportunity can be best described in terms of the well-known Moore's law for the progression of the feature size in CMOS electronics with time, as depicted in the figure below.



Let us focus on the three important length scales in this figure. The first length scale is the de Broglie wavelength of electrons in Silicon. It is ~ 10 nm and is a measure of the ultimate limit to the feature size before one enters the quantum regime. The second fundamental length scale, one that has not received much attention in the Silicon world, is the photon wavelength in the semiconductor. This length scale is important because it is a measure of the ultimate limit to the size of the nanophotonic devices in much the same way that the electron wavelength sets the limit for the CMOS electronic feature size. The third important length is the 90 nm feature size in the CMOS production fabs in

2004. This provides an unprecedented opportunity of enabling Silicon nanophotonics, and by extension for EPICs, as discussed below.

Although the photon wavelength is a measure of the ultimate limit on the size of a photonic device, the current photonic devices are considerably larger (x20,000 longer in length in some cases). This is because radiation losses at the bends in the waveguides provide the ultimate loss mechanism once the absorption and scattering losses are made negligible. Large bend radii (and hence large device/circuit size) are, therefore, required to avoid radiation losses for the small refractive index contrast (~ a few percent) materials currently used for photonic devices and circuits. High (> 2:1) index contrast Si/SiO₂ waveguides would enable wavelength-scale nanophotonic devices and circuits, but only if roughness-induced scattering losses, which increase strongly with increasing index contrast, can be minimized. The emerging 90 nm CMOS fab lines provide the smoothness necessary for reducing the scattering losses and thus ultimately enabling wavelength-scale nanophotonic devices not heretofore possible. This presents an unprecedented opportunity of fabricating VLSI nanophotonics on Si in a process compatible with CMOS processing.

Once it becomes possible to fabricate high performance photonic and optoelectronic circuits in a CMOS compatible process in Silicon, the obvious next step is to integrate CMOS electronics on the same chip, leading to high performance VLSI nanophotonics and electronics on a single Silicon chip. Such EPIC chips can enhance the functionality of photonics (e.g. by making photonic circuits more adaptive to environment, making modulators faster, and less power hungry by having driver electronics right next to the modulators, controlling the relative phases of different arms of the circuit etc.). Such EPIC chips may also enhance electronic circuits, for example by providing a better clock distribution system. Another major advantage is that a single, well-developed monolithic platform used for the EPIC chips will replace the multiple material and processing platforms used currently to achieve the required photonic and electronic functions. All of these advantages, coupled with reduced size, power and cost, will provide a powerful impetus for diverse DoD and commercial applications of EPIC chips at the intersection of photonics and electronics. This is the vision for EPIC, the new program DARPA is about to launch.

There are three major challenges that have to be met in order to realize this vision: (1) Demonstration of a complete suite of high speed, high performance nanophotonic devices, fabricated in a CMOS compatible process, (2) Integration of nanophotonic devices and electronics on the same Silicon chip and demonstration of some VLSI EPIC chips for specific applications, (3) development of the missing photonic devices, such as a laser, amplifier, and wavelength converter, in a CMOS compatible technology. Although the technology for electronic circuits for drivers, trans-impedance amplifiers etc. is well established, putting multiple units of these together on a single chip will require careful design and is a non-trivial challenge.

We believe that EPIC has the potential to revolutionize the intersection of photonics and electronics. EPIC chips will find ubiquitous applications, inn

communications, sensors, RF photonics, and wherever photonics and electronics intersect. The solicitation is expected to be announced in January 2004 and a link to it can be found under solicitations on the MTO web page (www.darpa.mil/mto).

POC:

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